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Junctionless Transistors for Future Applications

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ABSTRACT

A study of junctionless transistors is discussed in the paper. With the need of smaller dimension of the transistor for modern technology, the complexity of the formation of abrupt source/drain junction with the channel, the leakage current, and the short channel effects (SCEs) are increasing. Junctionless Field effect transistor (JLFET) technology may be the solution to this problem. The short channel effects (SCEs) are improved in the JLFETs and also the fabrication of JLFETs is easy at lower dimensions as it does not contain any source/drain junction with channel.

Keywords: *Junctionless transistors, depletion layer, short channel effects, filed –effect transistors, threshold voltage.*

1. INTRODUCTION

Junction less nanowire transistor (JNT), developed at Tyndall National Institute in Ireland, is a nanowire based transistor that has no gate junction. Junctions are difficult to fabricate, and because they are a significant source of current leakage, they waste significant power and heat. Eliminating them held the promise of cheaper and denser microchip. The JNT uses a simple nanowire of silicon surrounded by an electric ring that acts as a gate and controls the flow of electrons through the wire.

A junction less Transistor is an attractive device due to its simple process architecture without concerning thermal budget in the formation of source and drain junction [1]. In a junction less transistor (JLT) since it is uniformly doped device throughout with N+ silicon nanowire for p-channel MOSFET so it has no source and drain junction. So, it is an accumulation mode device with heavy doping concentration of either donor type for n-channel JLT or acceptor doping for p-channel JLT.

2. DEVICE FABRICATION

The key to fabricating a high-performance JNT is the formation of a semiconductor layer that is thin and narrow enough to allow for full depletion of carriers when the device is turned off. The semiconductor also needs to be heavily doped to allow for a decent amount of current flow when the device is turned on. The JLT is a silicon nanowire surrounded by gate stack materials in what becomes the channel region. It has a constant heavy doping concentration through source, channel and drain (N-type in an n-MOS device and p-type in a p-MOS device). It can be considered as a gated resistor with uniform doping[2].

The use of such a structure automatically eliminates impurity diffusion-related problems [3].Despite presenting a structure similar to that of accumulation mode transistors(N+-N-N+)[4], JL devices are different from Accumulation mode devices in that, in the on-state, conduction only occurs in the bulk(centre) of the nanowire ,and that no surface accumulation layer is formed.

This is related to the higher channel doping concentration of JLT with respect to the accumulation-mode devices, which induce the former to operate mostly in partial depletion, whereas the latter starts to operate in accumulation just after the threshold [5].

3. CONDUCTION MECHANISM

The Junction less transistor is basically an on-device where the work function difference between the gate electrode and the silicon nanowire shift the flatland voltage and the threshold voltage to positive values Below threshold, the junction less channel is depleted of electrons and the current varies exponentially with gate voltage (Fig.2a). At threshold, a natural silicon filament forms between sources and drain (Fig.2b).

The cross-section of filament increase, when gate voltage is increased (Fig.2c) until depletion disappears and the device is in flat bond condition (Fig. 2d).

When the device is turned off (Fig. 2a), the effective channel length , distance between the non- depleted source and drain region varies from a distance less than the physical gate length in the centre of the nanowire to a distance larger than the physical gate length near the peripheral of the nanowire [6] .

The physics of the JNT is quite different from that of standard multi-gate FETs. Depletion of the heavily doped nanowire creates a large electric field perpendicular to current flow below threshold but above threshold the field drops to zero. This is the opposite of inversion-mode (IM) or even accumulation-mode (AM) devices where the field is highest when the device is turned on.

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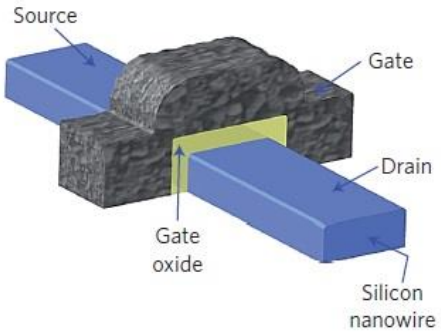

Fig1. Schematic of an n-channel nanowire transistor

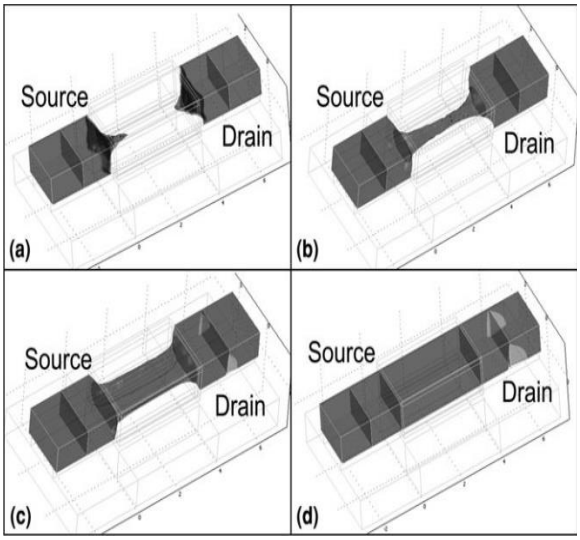

Fig2. Conduction mechanism

The device is turned off not by a reverse-biased junction, as in case of conventional MOSFET, but by full depletion of the channel region. This depletion is caused by the workfunction difference between the gate material and the doped silicon in the nanowire.

The Fig. 3 shows the energy band diagram of n-channel JNT, assuming a p+ polysilicon gate electrode. Flat band condition is achieved when a positive gate bias is equal to the workfunction difference between the nanowire and the gate material is applied to the gate (Fig. 3A).In that case the device is turned on. When a zero gate bias is applied, the channel region is fully depleted (Fig. 3B).

The threshold voltage of JNT depends on doping concentration, nanowire thickness and width.

The drain current of the JNT is proportional to the channel doping concentration and the cross section of the nanowire ,and not to the gate-oxide capacitance.

4. SINGLE MATERIAL AND DUAL MATERIAL JLFETs

The JLFETs may have single material double gate or double material double gate. The carrier mobility, transconductance and short channel effects are improved in dual material gate[7]-[11].Dual material gate has higher drain current than the single material gate(SMG)devices, and there is a step in a surface potential because of difference in the work functions of gate materials, an enhanced electric field in the channel[7],[8].The dual material gate structure also reduces the peak electric field near the drain and a smaller peak arises near the source region, which provides more acceleration to mobile charge carrier (electrons), and therefore carrier velocity is increased[7].

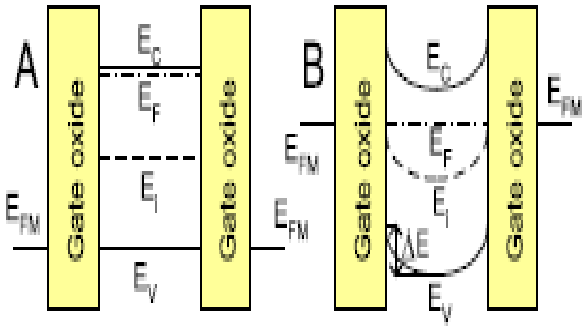

Fig.3 The energy band diagram of a n-channel JNT in (A) flat-band condition (the device is turned on) and (B) in the off state (the channel region is fully depleted).

Dual material concept is widely used in the MOSFET[9],[10] for reduced SCEs. The concept is also valid for the JLFETs structures. The JNT with dual material gate has higher on state current than the SMG-JNT counterpart. The other desirable features are higher on-to-off current ratio, better transconductance, higher unity gain frequency etc. The electric field peak value near the drain is reduced for the DMG-JNT. The hot carrier effect (HCE) and SCEs are also observed to be reduced as the peak electric field is effectively reduced near the drain. When the threshold voltages are compared, it is observed that the dual material gate structure has lower threshold voltage than the single material gate structure.

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5. ADVANTAGES AND DISADVANTAGES

The complementary metal-oxide-semiconductor (CMOS) technology has recognized as dominant technology to achieve high speed, low power, high packing density and low cost digital logic as well as semiconductor memories due to continuous downsizing of metal-oxide field –effect-transistor(MOSFET).
Further, the advancement in CMOS technology has made it also attractive for system-on-chip(SOC) products too, where digital circuits and memories can also be integrated with the analog /RF circuits for ultra-high speed operation together with reduced system cost. For analog /RF circuits, major challenges in nanometer regime are short channel effects(SCEs) and stringent process requirements for formation of abrupt source/drain regions[12]-[15].The junctionless field effect transistor (JLFET) eliminates these requirements with improved SCEs and its simple structure makes fabrication process easier[14].In spite of these advantages, JLFETS suffer from mobility degradation due to highly doped channel which also affects the transconductance (g_m) or gain ,as a result poor ON current ,hence, inferior analog /RF performance as compared to counterpart MOSFETs[16].

6. APPLICATIONS

Junctionless transistor is a promising candidate for electronic circuit and communication system.JNT inverter based ring oscillator can generate oscillation at low power supply and can be electrically tuned [17]. The double gate (DG) JL device does not require drain and source extension region engineering, can perform significantly better than conventional inversion mode devices and can be used for ultra low power application[18]. The concept of bipolar JL transistor can also be utilized in designing an ultra-sensitive interface for future sensing application.

7. CONCLUSION

This paper presents a comprehensive study of junctionless transistor. The junctionless nanowire transistor is a novel multiple gate device containing no distinct p-n junction in its structure. The fabrication of device, its working mechanism and its types are briefly discussed. JNT is a strong contender for future CMOS. Its multi-gated structure can be exploited for better gate control against the short channel effects. The presence of the gate electrode on more than one side of the device effectively improves the electrostatic control over the channel. It has been also stated that JNT can exhibit low leakage currents and excellent short channel behavior at shorter gate lengths. JNT inverter based ring oscillator can generate oscillation at low power supply and can be electrically tuned. Junctionless transistor can be considered for communication system applications. JLT Compact Modeling is the most important future scope of it, which play a vital role in semiconductor industry.

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