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Optical Routers: A Comparative Study

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ABSTRACT

Due to the emergence of data centric applications the demand for more bandwidth has increased tremendously. To cater to such demand, optical packet switching (OPS) which heavily relies on very large bandwidth of optical fiber and WDM technology can provide very effective solution. In OPS, the design of optical switches (Routers) play vital role, and thus many designs have emerged in past. However, due to the complex nature of optical system each switch has their advantages and disadvantages. There are nearly countless attributes that affects the switch performance like; loss, noise, crosstalk, bit rate dependency, polarization dependent loss, buffering, packet loss rate etc., and it is nearly impossible to design a switch which can well under all these attributes. In this paper, design analysis three optical nodes architectures are detailed to analyze the effect of various attribute on switches. The analysis is carried out in terms of loss, power and noise analysis. The comparative analysis of the architectures is also done, and it is shown under various conditions different architectures perform differently.

Keywords: *FDL, FBGs, WDM, TWC, AWG, BPF*

1. INTRODUCTION

In the present day telecommunication environment the demand of internet traffic is growing very rapidly. In this growing environment the demand of higher bandwidth increases day by day due to the data centric applications like internet TV, Video on demand etc. In recent past, the fiber optical network has become the core of our telecommunication and data networking infrastructure. The Optical Packet/Burst switching are the major technologies which may be useful when building networks to cater to this increasing demand of bandwidth. The Optical Packet/Burst switching provides the high bandwidth utilization, low latency, and high throughput[1-2]. The implementation of optical network is composed of switches which are either all optical or can be electronic in nature. Main aim of the switching is to route the packet to its correct destination port. The major issue involved in optical network is to design of the switch, router architecture which can perform the switching operation effectively with high data rates. In the current technology, because of non feasibility of optical processor a mix approach is used where data propagates in the optical domain and control operations are performed by the electronics .This mix approach is referred as the photonic packet switching technology. [3-4].

One of the major drawbacks of Optical Packet Switching and Optical Burst Switching technology is the un-availability of optical RAM [5-7]. Thus, as an alternative approach fiber delay lines (FDLs) are used for the storage of contending packets. In these FDLs storage is very limited due to the physical layer constraints like dispersion, crosstalk and noise. Photonic packet switches are characterized as passive-buffered. Here, the passive-buffered implies that only passive fiber delay lines, such as fiber loops are used for the storage of packets. The common fiber delay lines optical buffer re-circulates the packets stored instead of holding them statically or stationary in as in RAM. It is also possible to store multiple packets in a single fiber loop using WDM technology.

Due to noise accumulation in the fiber loop delay lines, the depth of the fiber loop memory limited to some number of re-circulations [8]. This clearly implies that it is not possible to store more than a limited number of packets in common shared buffer. The noise and crosstalk accumulation inside the fiber loop is proportional to the number of wavelengths used to store the packets inside the buffer. This causes a limitation on the number of wavelengths that can be used in the fiber loop. These considerations imply that photonic switches will need algorithms that use buffers efficiently, in accordance with the inherent limitations of the switch. Due to the limited number of re-circulations of the contending packets inside the buffer, available buffer may not be fully utilized. Thus it is necessary to use cross layer optimization which integrates the physical and networks layers parameters for proper utilization of the resources in designing optical switched based networks.

The generic layout of the optical network along with core switches is shown in figure 1. In packet switching, information is transmitted in the forms of optical packets and each packet contains header and payload [9]. Header contains information like the address of source and destination, and processed at each switch in the network (usually called core routers). The Edge routers placed at the periphery of the network has optical to electrical and electrical to optical conversion capability, and packet aggregation also takes place. The optical packet switching system is designed for optical cloud only. As in this cloud very high speed data propagates with lot of information stored in a packet, thus packet loss should be kept as minimum as possible. Therefore, in case of contention, a process when more than one packet try to occupy the same outgoing link, as a one possible solution except one other contending packet

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will be buffered. This buffering is made possible by incorporating components such as optical couplers, optical amplifiers AWG router and tunable wavelength converters. However, because of the large physical loss of the switches, generally optical amplifier is placed anywhere in the switch to compensate the loss. This amplifier re-stores the signal power, but adds ASE noise to the signal. Also other unwanted phenomenon crosstalk happens from one channel to another. The effect of noise can be relaxed by using higher power levels, but at higher power levels non linear effect is start to dominate and phenomenon of Four-Wave Mixing (F.W.M) affects the system performance drastically. Thus even high power does not provide very effective solution. Thus design of an OPS node with low insertion loss and very low packet loss is desirable.

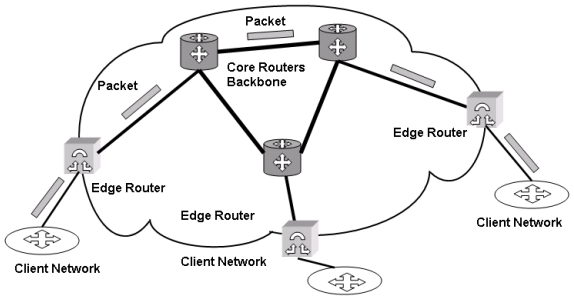

Fig. 1: Generic layout of the Optical Network

In this paper, three optical packet switches are compared in detailed and it is shown that a single design cannot be used every where, in different circumstances different architectures perform well.

This paper is organized as follows, in section 2; description of the architectures is presented. In section 3, mathematical analysis is done to obtain the loss, power and noise and finally BER. The calculations and results of the paper are presented in section 4 of the paper. The major conclusions of the paper are presented in section 5 of the paper.

2. ARCHITECURES DESCRIPTION AND ANALYSIS

In this work three optical packet switches are compared in terms of power budget, components analysis and network layer performance parameter packet loss probability. The switches presented here, designed for equal length packets and packets arrive synchronously at the input of the switch [10]. This synchronization is necessary for the correct operation of the switch. In this section a brief description of the three architectures is detailed. The three architectures are classified as A1, A2 and A3.

Architecture A1

The schematic of the switch design is shown in figure 2. Here, TWCs placed at each input of switch are tuned to place the incoming packets either in the buffer or to pass them directly towards outputs. Considering a 4 output switch as shown in Figure 3, here packet can be directly transmitted to output 1 to 4 at wavelength λ_1 - λ_4 respectively. TWCs in branch 2 converts λ_9 - λ_{12} to $\lambda_5 - \lambda_8$. TWCs in branch 1 will convert λ_5 - λ_8 to λ_1 - λ_4 . Thus packets are accepted at outputs, and packets on these wavelengths get blocked in the buffer as BPFs will not allow these wavelengths to pass.

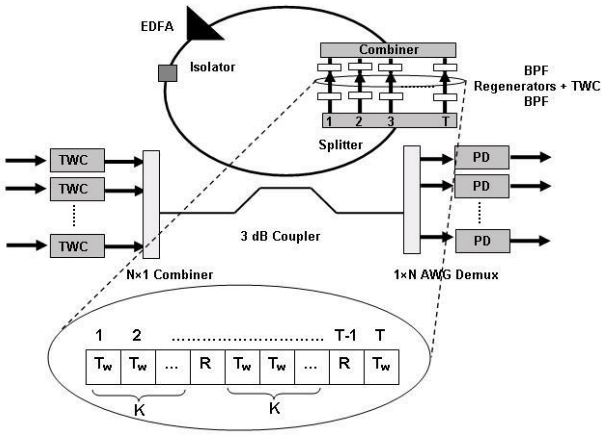

Fig. 2: Schematic of architecture A1

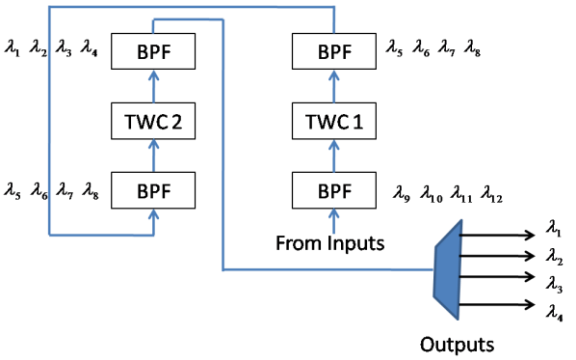

Fig. 3: Buffering concept of architecture A1

In the buffer, the combination of regenerators and TWC's can be placed in such a way that packets get regenerated before the upper circulation limit (K) is reached. For the regeneration, packet inside the buffer gets assigned to any one of the regenerator wavelength (λ_R), and gets regenerated. The re-circulation limit will decide the number of regenerators that have to be placed in the buffer, so that no packet remains in the buffer for more than K circulations without regeneration. In the loop buffer, multi-wavelength 3R regeneration is assumed [11]. The 3R regeneration removes the circulation limit, and data can again stay in the buffer for K circulations [11]. Thus by regenerating data again and again packet can be kept for the large duration in the buffer.

Required number of regenerator for different buffer size and circulation limit can be obtained by using simple formula $R = \lceil T / K \rceil - 1$ or 0 whichever is large.

Architecture A2

Architecture A2 is the modified version of the architecture A1, where direct path is very much similar to architecture A1, however buffer unit is simplified significantly.

Considering a $N \times N$ i.e., N inputs and N outputs switch, the FBG marked as '0' reflects wavelength λ_1-λ_N without any delay, and received by output 1 to N respectively. Buffer wavelength ranges from λ_{N+1} - $\lambda_{(B+1)N}$ as shown in Fig. 4. In the buffer, sets of FBGs are placed, and between consecutive gratings fiber delay line of half of the slot duration is added [12]. These delay lines provide delay of integral multiple of slot duration as each packet pass through each delay line twice, once in forward direction and once in backward direction after getting reflected from the grating. Total number

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of wavelengths used by the switch is $T = (B+1)\,N$. The number of TWCs at the input of the switch is always equal to N, but number of FBGs inside the buffer will depend upon higher layer parameters like packet loss probability/average delay etc and can be greater or less than N.

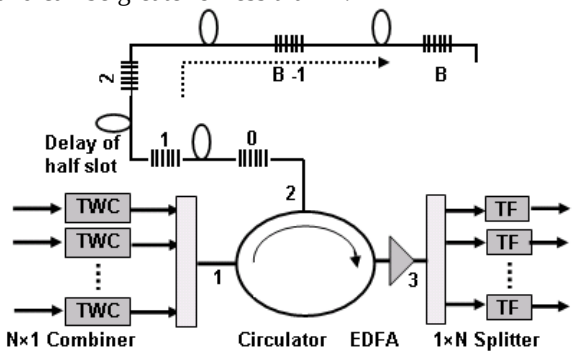

Fig. 4: Schematic of architecture A2

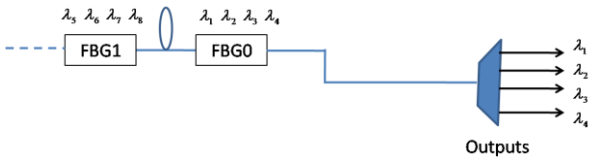

Fig. 5: Buffering concept of architecture A2

Considering, 4 redix switch as shown in Figure 5, here packet can be directly transmitted to outputs 1 to 4 at wavelength λ_1 - λ_4 respectively getting reflected from FBG0. FBG1 reflects packets at wavelengths $\lambda_5 - \lambda_8$ which are accepted by outputs after a delay of one slot. Thus depending on wavelengths, packets received at the output after definite amount of delay.

Architecture A3

In architecture A3, switch is further simplified; here both input/output and buffering units are simplified significantly.

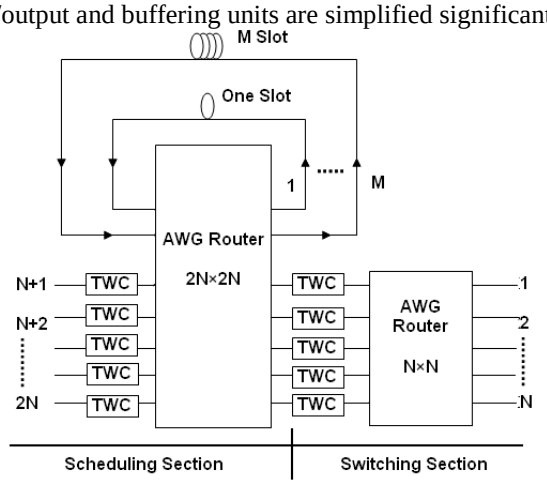

Fig. 6: Schematic of architecture A3

The architecture (Fig. 6) consists of both scheduling and switching section for the contention resolution of the packets. The core of the scheduling section is a $2N\times2N$ AWG router, and that of switching section is an $N\times N$ AWG router. The upper N ports of the AWG router of the scheduling section ranging from 1 to N are used for connecting N buffer modules. The lower ports of the AWG act as actual inputs/outputs port of the switch [13].

Packets wavelengths are selected appropriately by following the routing pattern of AWG, either to place them in buffer or to direct them towards the outputs.

In each buffer module, we can store N packets; one on each N wavelengths, with only one packet can be stored for a particular output port. Thus at most, N packets can be stored in all the modules for a particular output port. Hence, the length of the queue for each output port will be decided by the number of modules with maximum values of N packets.

3. POWER BUDGET ANALYSIS

The power budget analysis is necessary to identify the minimum power of the signal which passes through the switch and correctly identified at the switch outputs. In the power budget analysis following steps is followed:

1. Calculation of loss when signal passes through the switch
2. Gain estimation of EDFA
3. Total signal power received at the output.
4. Noises accumulation within and at the receiver of the switch.
5. Bit Error Rate analysis.
6. At a fix BER of $\leq 10^{-9}$, identification of minimum power levels for different switch and buffer combinations.

*Analysis for Architecture A*1

Loss Calculations

For the mathematical point of view the switch can be divided into three parts as input unit, buffer unit and output unit.

The loss of input unit which consists of TWC and combiner can be obtained as

$$A_{in} = A_{TWC} A_{Com}^{in} \tag{1}$$

The loss of loop buffer can be calculated by breaking the loop into two parts.

Let us consider loss from input of the 3 dB coupler to entry port to EDFA to be A_1 and that from the EDFA output to upto 3dB coupler to be A_2. The A_1 and A_2 are given by

$$A_1 = A_{3dB} A_{Split} A_{BPF} A_{TWC} A_{BPF} A_{Com}^{b} A_{F1} \tag{2}$$

$$A_2 = A_{ISO} A_{F2}$$

Here, A_{3dB} is loss due to 3dB coupler, A_{Demux}, A_{Com} and A_{TWC} are losses due to Demultiplexer, Combiner and Tunable Wavelength Convertor respectively. $A_F = A_{F1}A_{F2}$ is the total fiber loss and L_{Iso} is the isolator loss.

If data takes K circulations in the loop, then the total loss of the loop buffer can be written as $A_l = A^K$, where $A = A_1 A_2$ is the total loss of the loop buffer in one circulation.

Similarly, the loss of output unit which consist of coupler and AWG demux can be obtained as

$$A_{out} = A_{3dB} A_{AWG} \tag{3}$$

Here, the loss of 3dB coupler is considered because as data comes out of the loop buffer it again has to pass through the coupler.

By combing all the above losses, total loss of the switch can be written as

$$A_T = A_{in} A_l A_{out} \tag{4}$$

Since, the loss of the buffer unit is compensated by the EDFA, therefore the above loss equation can be written as,

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$$A_T = A_{in}\left(AG\right)^K A_{out} \quad (5)$$

Power Calculations

In this analysis power of the signal is computed after each circulation.

TWC as a transparent device

In this sub-section, TWC is assumed as a transparent device, means it tunes the wavelength of the incoming signal, without adding any noise to the signal.

Power entering the loop buffer for bit *b* is

$$P_s = bP_{in}A_{in}, \qquad b \in [0,1] \quad (6)$$

The extinction ratio ($\varepsilon = P_0/P_1$) is assumed to be zero. The signal power after one circulation is

$$P_s(1) = P_s AG_1 + n_{sp}\left[G_1 - 1\right]h\nu B_0 A_2 \quad (7)$$

If we assume that the data remain in the buffer for *K* circulations. Then TWC inside the buffer will remain transparent for first $(K\text{-}1)^{th}$ circulations and tunes the wavelength in the K^{th} circulation. Thus the power of the signal after *K*-1 and *K* circulations for bit *b* is given by

$$P_s(K-1) = P_s\left(K-2\right)AG_{K-1} + n_{sp}\left[G_{K-1} - 1\right]h\nu B_0 A_2 \quad (8)$$

And

$$P_s(K) = P_s\left(K-1\right)AG_K + n_{sp}\left[G_K - 1\right]h\nu B_0 A_2 \quad (9)$$

respectively.

The term P_s (*K*-1) is the signal power just before the 3dB coupler in the beginning of the K^{th} circulation, G_K is the gain of EDFA in K^{th} circulation and the term $n_{sp}[G_K\text{-}1]h\nu B_0$ represents the ASE noise power added to the signal in the K^{th} circulation [14].

The power for bit *b* at the output of switch is

$$P_{out}(K) = P_s(K) \times A_{out} \quad (10)$$

The above equations can be simplified by considering that the gain of the EDFA is flat with respect to wavelengths in the region of interest (1530-1570 nm), thus constant gain *G* in each circulation can be assumed. Therefore, the equation 9 can be written in modified form as

$$P_s(K) = bP_{in}A_{in}\left(AG\right)^K + n_{sp}\left(G-1\right)h\nu B_0 A_2 F \quad (11)$$

Where

$$F(K) = \begin{cases} \dfrac{1-(AG)^K}{1-AG} & AG \neq 1 \\ K & AG = 1 \end{cases}$$

For the maximization of *SNR* the gain loss product (*AG*) should be equal to one [12], equation 11 can be simplified as

$$P_s(K) = bP_{in}A_{in} + n_{sp}\left(G-1\right)h\nu B_0 A_2 K \quad (12)$$

and power at the output of the switch is

$$P_{out}(b) = P_s(K)A_{out} \quad (13)$$

B. Analysis for Architecture A2

1) Loss Analysis

The loss of the input which consists of TWC and combiner is $A_{TWC}A_{Com}^{N\times 1}$, the loss of output unit which consists of splitter and TF is $A_{FBG}A_{Cir}A_{Spt}^{1\times N}A_{TF}$, and the loss of buffer unit is BA_{FBG}.

The maximum possible loss when a packet passes through the switch is

$$A = A_{TWC}A_{Com}^{N\times 1}(B+1)A_{FBG}A_{Cir}A_{Spt}^{1\times N}A_{TF} \quad (14)$$

This loss is compensated by EDGA, and the condition *AG*=1 is maintained which maximizes the SNR [8].

Power Analysis

Again, power entering in buffer module for bit *b* is

$$P_s = bP_{in} \qquad b \in [0,1] \quad (15)$$

The extinction ratio ($\varepsilon = P_0/P_1$) is assumed to be zero.

Power at the output of the switch is

$$P_{out} = P_s + P_{sp}$$

$$P_{out} = bP_{in} + n_{sp}(G-1)h\nu B_0 A_{Spt}^{1\times N}A_{TF} \quad (16)$$

The term $n_{sp}(G-1)h\nu B_0$ represents the ASE noise of the EDFA amplifier.

C. Analysis for Architecture A3

The loss of the input unit which consist of TWC can be written as

$$A_{in} = A_{TWC} \quad (17)$$

The loss of the buffer can be calculated as

$$A_b = A_{AWG}^{2N\times 2N}A_{FDL} \quad (18)$$

Here, $A_{AWG}^{2N\times 2N}$ is loss due to the scheduling AWG. A_{FDL} is the loss due to the fiber delay lines.

Similarly, the loss of the output unit which consist of the switching and scheduling AWG and TWC can be obtained as

$$A_{out} = A_{AWG}^{2N\times 2N}A_{TWC}A_{AWG}^{N\times N} \quad (19)$$

Now by combining all the above equations 17-19, the total loss of the switch can be written as

$$A_T = A_{in}A_bA_{out} \quad (20)$$

Power Analysis

In the sub-section power analysis is presented. Power entering in buffer module for bit *b* is

$$P_s = bP_{in} \qquad b \in [0,1] \quad (21)$$

The extinction ratio ($\varepsilon = P_0/P_1$) is assumed to be zero. Power at the output of the switch is

$$P_{out} = P_{in}A_T \quad (22)$$

Noise analysis

These noise components generated at the receiver are shot noise, ASE-ASE beat noise, sig-ASE beat noise, shot-ASE beat noise and thermal noise variances are denoted by σ_s^2, σ_{sp-sp}^2, σ_{sig-sp}^2, σ_{s-sp}^2, and σ_{th}^2 respectively [14]. For the bit *b* the different noise components can be formulated as:

$$\sigma_s^2 = 2qRP_sB_e$$

$$\sigma_{sp-sp}^2 = 2R^2P_{sp}(2B_o - B_e)\frac{B_e}{B_0^2}$$

$$\sigma_{sig-sp}^2 = 4R^2P_s\frac{P_{sp}B_e}{B_0}$$

$$\sigma_{s-sp}^2 = 2qRP_{sp}B_e \quad (23)$$

$$\sigma_{th}^2 = \frac{4K_BTB_e}{R_L}$$

The total noise variance for bit *b* is

$$\sigma^2(b) = \sigma_s^2 + \sigma_{sp-sp}^2 + \sigma_{sp-sig}^2 + \sigma_{s-sp}^2 + \sigma_{th}^2 \quad (24)$$

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$$BER = Q\left(\frac{I(1)-I(0)}{\sigma(1)+\sigma(0)}\right) \quad (25)$$

$$Q(z) = \frac{1}{\sqrt{2\pi}}\int_{z}^{\infty} e^{-\frac{z^2}{2}} dz \quad (26)$$

Where, $Q(\cdot)$ is error function, and '*R'* is responsivity of the receiver. In BER, $I(1) = RP(1)$ and $I(0) = RP$ (0) are photocurrent sampled by receiver during bit '1' and bit '0' respectively.

4. CALCULATION RESULTS

Calculation:

Using the above formulation and the values of the parameters as given in Table 2, the results obtained in terms of BER for different architectures at different power levels for different buffering condition for fixed input switch size is presented in Table 3-7.

Table 1. AWG Specifications.

Specification	Value
Number of Channels	40
Channel Spacing	100 GHz
Operating wavelengths	ITU grid
Insertion loss	3.0 dB
Adjacent channel crosstalk	26 dB

Table 2. List of Parameters and Their Value [8,15].

Parameters	Value
Size of the switch (*N*)	4
Population inversion factor (n_{sp})	1.2
Loss of Circulator (A_{cir})	1.0 dB
Loss of Isolator (A_{Iso})	0.5 dB
Bit (*b*)	0,1
Speed of light	3×10^{8} m/s
Gain of the amplifier (*G*)	-
Loss of FBG	1.0 dB
Loss of BPF	1.0 dB
Loss of TF	1.0 dB
Responsivity (*R*)	1.28 A/W
Electronic charge (*e*)	1.6×10^{-19} C
Electrical bandwidth (B_e)	20GHz
Optical bandwidth (*Bo*)	40GHz
Temperature (*T*)	300K
Boltzmann Constant (K_B)	1.38×10^{-23}
TWC insertion loss (A_{TWC})	2.0 dB
Loss of splitter/combiner	6.0 dB
Loss of Scheduling and Switching AWG (32 channels) (A_{AWG})	3.0 dB
Loss of SOA (A_{SOA})	1.0 dB
Loss of Fiber (A_F)	0.2 dB/Km
Re-circulations (*K*)	-
Buffer (*B*)	4, 8

For switch A1, of redix 4, for the buffering capacity of 4 and 8 packets for each output, the BER at different power levels is presented in Table 3 and 4. It is clear from the table that as the power increases the BER performance of switch improves significantly. For the acceptable limit of BER$\leq10^{-9}$, the minimum power level is nearly 0.8 milli-watts. It can also be observed from the table that due to the accumulated noise in each circulation, the BER performance degrades. In Table 4, BER performance is shown for the buffering capacity of 8 packets. Here of the acceptable BER, the minimum amount of required power is 4 milli-watts which is 5 time higher compare to the buffering of 4 packets. Thus, in this design if storage is increased then rise in power is huge.

For switch A2, of redix 4, for the buffering capacity of 4 and 8 packets for each output the BER at different power levels is presented in Table 5 and 6. Again similar trends are obtained and as power increase the BER performance improves. For the buffering of 4 packets the required amount of power is 300 nano-watts which increase to 700 nano-watts for the buffering of 8 packets. Thus, in architecture A2 in comparison to architecture A1, the required amount of power is very less.

The third architecture A3 is AWG based over here the minimum power required for the satisfactory switch operation is 7 microwatts. Thus, overall in terms of power requirement the architecture A2 perform best.

It must be remembered that, as the switch size increase the losses in architecture A1 and A2 increases exponentially. Hence for switch redix greater than 4, the switch architecture A3 performance will be much superior to A2. The performance of architecture A1 is poorest among the three discussed designs.

Table 3. Architecture A1: Switch Size 4×4, and Buffer 4.

Power in milli-watts	Circulation Count	BER
0.7	1	6.06×10^{-30}
	2	7.15×10^{-16}
	3	3.97×10^{-11}
	4	9.82×10^{-9}
0.8	1	5.63×10^{-34}
	2	6.59×10^{-18}
	3	1.73×10^{-12}
	4	9.10×10^{-10}

Table 4. Architecture A1: Switch Size 4×4, and Buffer 8.

Power in milli-watts	Circulation Count	BER
3.5	1	3.07×10^{-37}
	2	1.61×10^{-19}
	3	1.43×10^{-13}
	4	1.41×10^{-10}
4.0	1	2.67×10^{-42}
	2	4.58×10^{-22}
	3	2.81×10^{-15}
	4	7.29×10^{-12}

Table 5. Architecture A2: Switch Size 4×4, and Buffer 4.

Power in nano-watts	BER
100	0.0018
200	1.36×10^{-6}
300	5.63×10^{-10}
400	3.03×10^{-13}
500	1.1×10^{-16}
600	3.55×10^{-20}
700	1.05×10^{-23}
800	2.89×10^{-27}
900	7.52×10^{-31}
1000	1.86×10^{-34}

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Table 6. Architecture A2: Switch Size 4×4, and Buffer 8.

Power in nano-watts	BER
100	0.041
200	0.0015
300	6.53×10^{-5}
400	2.57×10^{-6}
500	9.67×10^{-8}
600	3.55×10^{-9}
700	1.27×10^{-10}
800	4.5×10^{-12}
900	1.56×10^{-13}
1000	5.34×10^{-34}

Table 7. Architecture A3: Switch Size 4×4, 8×8, 16×16and Buffer 4, 8, 16.

Power in micro-watts	BER
1	0.11
2	0.00054
3	1.82×10^{-4}
4	4.48×10^{-6}
5	8.83×10^{-8}
6	1.45×10^{-9}
7	2.07×10^{-11}
8	2.61×10^{-13}
9	2.98×10^{-15}
10	3.11×10^{-17}

The major pros and cons of the three architectures are presented in Table 8.

Table 8. Comparative Study of the Architectures

	A1	A2	A3
Buffering Capacity	Can be varied by adjusting the re-circulations	Fixed	Fixed
Power Requirement	Maximum ~mW	Minimum ~nW	Moderate ~µW
Scaling of Buffer	Complicated: a large number of components needed	Moderate FBGs are required	Simple Only fiber pieces are needed
Physical Loss	Highest	Moderate	Lowest
Noise Accumulation	Severe	Moderate	Very Less
Effect of Fiber Non-Linearity	Yes	No	No
Multi-wavelength buffering capacity	Yes	Yes	Yes

5. CONCLUSIONS

Optical packet switching is considered as one of the more promising technology for the next generation high speed data transfer. In the similar context, in this paper, three optical packet switches are compared in terms of their functionality and power requirements. All the presented three architectures have their advantages and dis-advantages. Architecture A1 is most power hungry, while A2 is least power hungry. Form the paper following conclusions can be made:

- Architecture A1 is more power hungry, but it provide adjustable delay when packets are stored. Hence, this architecture is useful when adjustable delay is required.
- The presented switch A2 can operate in sub-micron power levels, thus most power efficient. However it provide limited buffer. Useful in very low power applications.
- Architecture A3 operates in micro-watts power regime and buffer is nearly lossless. This architecture is useful when high quality transmission is required.

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