Fast and Robust Real-Time Face Detection System using FPGA-based General Purpose Fuzzy Processor

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ABSTRACT

It is very challenging to recognize a face from a stream of images or real time frames from camera due to the wide variety of face and the uncertain of face position. This paper presents a novel and fast hardware architecture for face detection based on fuzzy rule based system using a fast FPGA-based general purpose fuzzy processor [1]. The proposed fuzzy system models the skin color distribution in YCbCr color space. The parallel processing which FPGA is described is used to accelerate the processing speed of the face detection system. The proposed architecture for face detection has been designed using VHDL language and Xilinx System generator in MATLAB and implemented by XtremeDSP Video Starter kit – Spartan 3A Development Kit. Experimental results demonstrate that our system has achieved high detection rates and low false positives over a wide range of facial variations in color, position and varying lighting conditions in both still image and real-time system.

Keywords: *FPGA, VHDL, video starter kit, Fuzzy Processor, Xilinx System Generator, Face Detection*

1. INTRODUCTION

In today's industry more and more automation is being introduced, which is a necessity to compete with countries with cheaper labor. In many of these automation solutions, where items need to be grasped or quality checked, computer vision play a great role. Normally these computer vision systems are implemented using a typical PC. Using a PC for the job is easy, as it has been done for many years, and therefore the technology is widely known. But when it comes to performance, the PC (mainly the Central Processing Unit (CPU) inside) is not necessarily the right choice. As the complexity of a vision system increases, the frame rate at which the PC is capable of processing images real-time decreases. This is due to the sequential operation mode of the CPU. Many of the demanding tasks of a vision system are trivial low level algorithms, where the same instructions are applied to each pixel in the frame. In this paper, low level algorithms could be implemented more efficiently on a parallel structure such as the Field Programmable Gate Array (FPGA). [2].

Face detection in image sequence has been an active research area in the computer vision field in recent years due to its potential applications such as monitoring and surveillance, human computer interfaces, smart rooms, intelligent robots, and biomedical image analysis [3]. And skin color has proven to be a useful and robust cue for face detection, localization and tracking. Some color spaces have been submitted in literature for face detection applications, for instance RGB, normalized RGB, HSV, and YCbCr. This kind of approach seem to be simpler and easier to implement, however they lack the robustness against illuminations, color bias of image acquisition device and other factors. To overcome this drawback, the color balance algorithm has been suggested. Considering the YCbCr color space, a human skin color model can be considered practically independent on the luminance and concentrate in a small region of the Cb-Cr plane [4].

Fuzzy sets theory has been successfully applied to many image processing and pattern recognition problems. Fuzzy techniques offer a non-linear and knowledge driven framework for coping with the ambiguity and vagueness often present in digital images, associated mostly with the definition of various elements such as edges and regions, or faces. Defining a suitable membership function to describe an image property is not a trivial task, since it depends on various factors that introduce different types of uncertainties, which finally translate into additional uncertainties about the membership function itself. Therefore, we must carefully seek more flexible, or even intuitive, ways in order to model uncertainty [5].

In the designing of fuzzy processor on FPGA, it should be noticed that there are big different between the designing of fuzzy controller and fuzzy processor. The difference can be presented as the fuzzy controller is programmed for a specific problem but the fuzzy processor is programmed for general purpose applications. It means that the fuzzy controller, the VHDL code is programmed for a specific problem with fixed inputs and outputs, and fixed rules. Also when it is wanted to change the fuzzy controller for another application, the VHDL code should be reprogrammed to be suitable [6]. On the opposite of the fuzzy processor can be suitable for many applications by changing some parameters for it without changing the VHDL code on FPGA [7].

In this paper, pixel-based skin detection method using fuzzy rule based system is proposed to classify each pixel to skin or non-skin pixels and YCbCr color space is chosen because of its good clustering properties. The fuzzy

rule based system is generated based on distribution of skin color in YCbCr color spaces. The Fuzzy rules will discriminate between skin and non-skin pixels. This paper is organized as follows: section 2 is about the some details about the designed general purpose fuzzy processor. Section 3 describes the usage of the proposed fuzzy rule base system for skin color segmentation in YCbCr Color Space and implementation of the proposed system using Xilinx System Generator. Section 4 describes experimental results of applying the proposed method and comparisons of its performance are presented.

2. PROPOSED FUZZY PROCESSOR ARCHITECTURE

The general purpose fuzzy processor architecture which it was designed and implemented in [1] is described as high-speed fuzzy processor and it successfully applied parallel-pipeline architecture and implemented with no-time-consumption rule identification. The general architecture of the proposed fuzzy processor is shown in Fig. 1, which has the characteristic parameters shown in Table.1. This proposed

fuzzy processor is divided into some sections as follows:

- Fuzzification Process.
- Active Rules Address Generator,
- Rule Inference Process, and
- Defuzzification Process.

These sections are all based on a set of membership functions. For more details about each stage in [1].

A. Implementation of the Fuzzy Processor

The main objective of this section is to design a general purpose fuzzy processor and implement it on an FPGA. The whole design is divided into four phases, each of which will be implemented using a top-down approach. All the circuits are coded in VHDL and simulated using ModelSim. Xilinx ISE is used for synthesis and implementation of the circuit on the FPGA board. This phase gives a high level description of the Fuzzy Processor (FP).
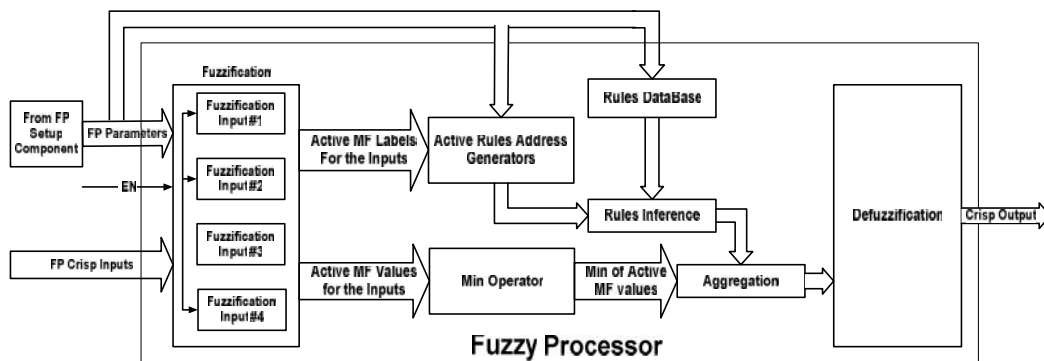

Fig.1: The proposed fuzzy processor architecture

Table 1: The proposed Fuzzy Processor Characteristics

Fuzzy Inference System	Mamdani FIS
Inputs	4
Input Resolution	8-bit
Outputs	1
Output Resolution	8-bit
Antecedent Mf's	8 Trapezoidal per fuzzy set
Antecedent MF Degree of Truth Resolution	8-bit
Consequent MF's	8 Trapezoidal per fuzzy set
Consequent MF Degree of Truth Resolution	8-bit
Aggregation Method	MAX
Implication Method	MIN
MF Overlapping Degree	2
Defuzzification Method	Center of Gravity (COG)

The FP is designed using the concept of fuzzy logic to get the output. Considering the FP to be designed as a black box, the inputs and outputs of the subsystem have been enlisted. A black box representation of the system is shown below in Fig.2, which enlists the inputs and outputs without
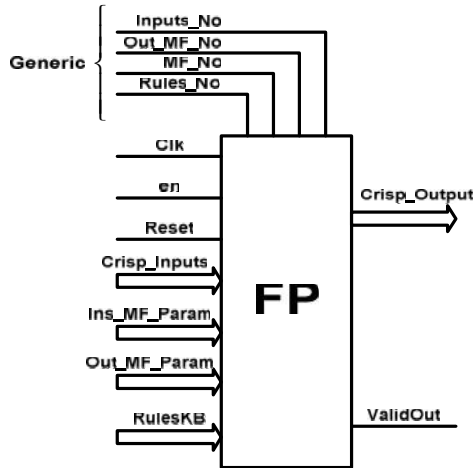
going into the gate level details of the subsystem and the synthesis report, which is generated from ISE WebPack program when the code is designed and implemented on xc3sd3400a-4fg676 chip in XtremeDSP Video Starter kit is shown in Fig.3.

In VHDL code, it is allowed to make some of parameters and the inputs width and some signals in the program depends on these parameters. These parameters are called generic inputs. It is chosen in this paper as follows:

Number of inputs (inputs_No), Number of Membership functions for each inputs (MF_No), Output Membership function Number (out_MF_No) and The number of rules (Rules_No) and some of inputs width depends on these generic inputs. The VHDL code which describes the inputs and the output is shown in Fig4.

Fig.2: Black box representation of designed fuzzy processor.

Fig.3: The synthesis report from ISE webpack program.

Device Utilization Summary				[-]
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	326	47,744	1%	
Number of 4 input LUTs	413	47,744	1%	
Number of occupied Slices	371	23,872	1%	
Number of Slices containing only related logic	371	371	100%	
Number of Slices containing unrelated logic	0	371	0%	
Total Number of 4 input LUTs	565	47,744	1%	
Number used as logic	413			
Number used as a route-thru	152			
Number of bonded IOBs	69	469	14%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	2.82			

After the implementation of our FP on FPGA through HW-Cosim in Xilinx System Generator is succeeded, we get that our fuzzy processor meets our design requirements in terms of speed, flexibility, and feasible implementation on FPGA board.

The next step is that the ability to apply it for face detection in real-time. The features implemented to make it variously configurable also make it applicable as a general-purpose fuzzy processor. Users can configure the fuzzy processor differently in terms of number of input variables, shape of input membership functions, minimum inference operations, and the shape and number of output memberships.

```
entity FuzzyController is
    generic (
            Inputs_No  : integer;
            MF_NOs   : arr4_int;
            Out_MFNo : integer;
            RulesNo    : integer
    );
    Port  ( Clk              : in  STD_LOGIC;
            en               : in  STD_LOGIC ;
            Reset            : in  STD_LOGIC;
            Crisp_Inps       : in  STD_LOGIC_VECTOR (8*Inputs_No -1 downto 0);
            INs_MFs_Param  : in  STD_LOGIC_VECTOR (4*8*(MF_NOs(3)+MF_NOs(2)+MF_NOs(1)+MF_NOs(0))-1 downto 0);
            RulesKB          : in  STD_LOGIC_VECTOR((Inputs_No+1)*3*RulesNo -1 downto 0);
            Out_MFs_Param  : in  STD_LOGIC_VECTOR (4*8*Out_MFNo-1 downto 0);
            Crisp_Output     : out STD_LOGIC_VECTOR (15 downto 0);
            en_Reset         : out STD_LOGIC;
            Valid_out        : out STD_LOGIC
```

Fig.4 VHDL Code for Inputs/Outputs definition of Fuzzy Processor

3. THE PROPOSED FUZZY RULE BASE SYSTEM FOR FACE DETECTION

A. Color Space Selection

Color model selection is the primary step in the skin color classification. The RGB color space is the default one for most available image format and the other color spaces could be obtained from a linear or non-linear transformation from RGB. Most widely used color spaces for the skin detection include: basic color spaces (RGB, normalized RGB, CIE-XYZ), perceptual color spaces (HIS, HSV, HSL, TSL), orthogonal color spaces (YCbCr, YIQ, Yuv, YES), and perceptually uniform color spaces (CIE-Lab and CIE-Luv) [8].

In the RGB color space brightness and color information are coupled together, so it is not suitable for color segmentation under unknown lighting conditions. The transformation of RGB to perceptual color spaces is invariant to high intensity at white lights, ambient light and surface orientations relative to the light source. Hence, it has acceptable performance to model skin color, but it may not be suitable for real-time application because the output format used by digital camera or capturing equipment is usually either YCbCr or RGB. Therefore, to avoid the extra computation required in conversion, the YCbCr color model is utilized in this work, which has the advantage of separating intensity component (Y) from the chroma components (Cb and Cr) [9].

Since we use only Cb and Cr components of YCbCr color space, computational burdens are also reduced dramatically in YCbCr color space.
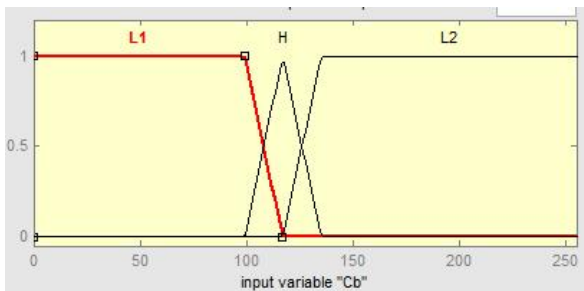
B. Skin Color Classification

After transforming the input image in to the selected color space, next step is searching the skin pixels, through the image. Although skin Colors are compact in CbCr Color Space, it still has small variances from person to person. If the

background color is similar to face-color, then we will have an additional problem for accurate detection of face-like regions. To overcome this problem, we try to capture the image region that is within certain values of Cb and Cr, i.e. try to detect the region that satisfies the condition (Cbmin<Cb<Cbmax and Crmin<Cr<Crmax). these threshold (Cbmin, Cbmax, Crmin, Crmax) values are sweeped through covering the whole possible face-CbCr values. Face-like regions are detected perfectly, if the correct threshold values are selected. When we select Cbmax=160, Cbmin=135, Crmax=125, Crmin=100, most of the skin regions are selected but with big false negative ratio [10].

In many applications, knowing that how much the color of a pixel acts like human's skin color is important also in the regions where color and non-skin colors overlapped , overlaps must based on an accurate measure determine that the desire pixel consider to which category. Since the effects of light on skin color segmentation should not disregard so a method is required which properly behave with different lighting conditions. To solve mentioned problems and resolve many other issues and enhance the accuracy and reliability, we used fuzzy method to skin color segmentation. In our method instead constantly assuming the threshold for each components we evaluate them by are class membership criteria. As follows that any of them how much acts close to the skin color defined values and then by combining the results of each one we will achieve to a unique answer that is membership degree for each pixel. In the other words determined that one pixel how much acts like color skin and how much is like non-color skin.

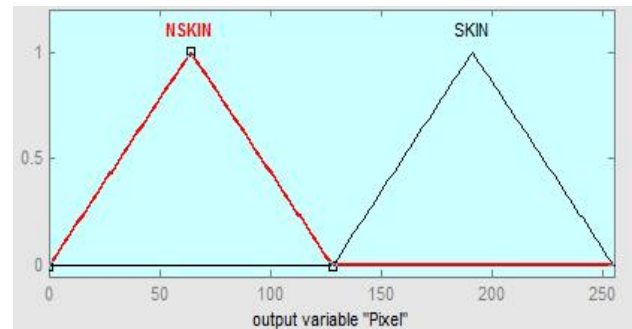## C. Fuzzy Inference for Skin Classifier

From the constant thresholds of each component of YCbCr color space as described before, it is noticed that the component Cb range which expresses on skin region between 135 and 160. Also with respect to Cr component between 100 and 125. Then, the skin region of each component is high in these ranges and other regions are low.Then, three fuzzy membership are made up to represent each variable's intensities; these sets are symbolized to the linguistic variables "L1", "H" and "L2" which denoting to low, high, low respectively. The adopted membership functions for the fuzzy sets of inputs and outputs are shown in Figure 5.

(a)
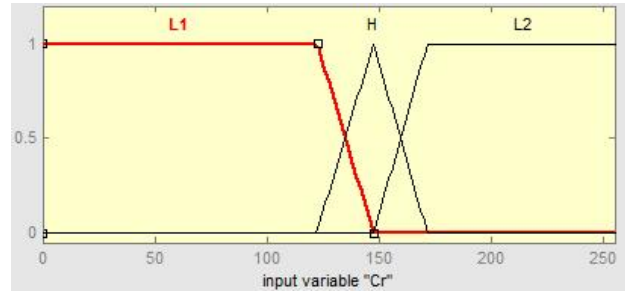
(b)

(c)

Fig. 5. "Fuzzy inference membership of skin classification:
a) Cb Input Memberships, b) Cr input Membership, and c) Output Membership of Pixel Value"

Table 2 describes the relationship between the inputs and the output in fuzzy rule base of the proposed fuzzy inference as follows:

Table2. Fuzzy Inference Rules

Cr Cb	L1	H	L2
L1	NSkin	NSkin	NSkin
H	NSkin	Skin	NSkin
L2	NSkin	NSkin	NSkin

4. EXPERIMENTAL RESULTS

To test and implement the proposed algoritm, two approachs are tested, the first approach test the algorithm on still image using hardware co-simulation by Xilinx system generator. The second tests the algorithm on real-time frames from the camera which is connected to the Xtreme Video Starter Kit.

A. Still-Image Test

100 images contain frontal, near frontal, and profile faces are selected to test the algorithm. These images are gathered among Bao and Caltech image datasets [11]. The method shows nearly acceptable result for near frontal faces. Figure.6 shows the model that uses the top level HDL module and its Xilinx Blocksets for face detection algorithm. This model can be used for co-simulation. Once the design is

verified, a hardware co-simulation block can be generated, and then will be used to program the FPGA for the proposed algorithm. Figure.7 shows the model with the hardware co- simulation block. The bitstream download step is performed using a JTAG cable.
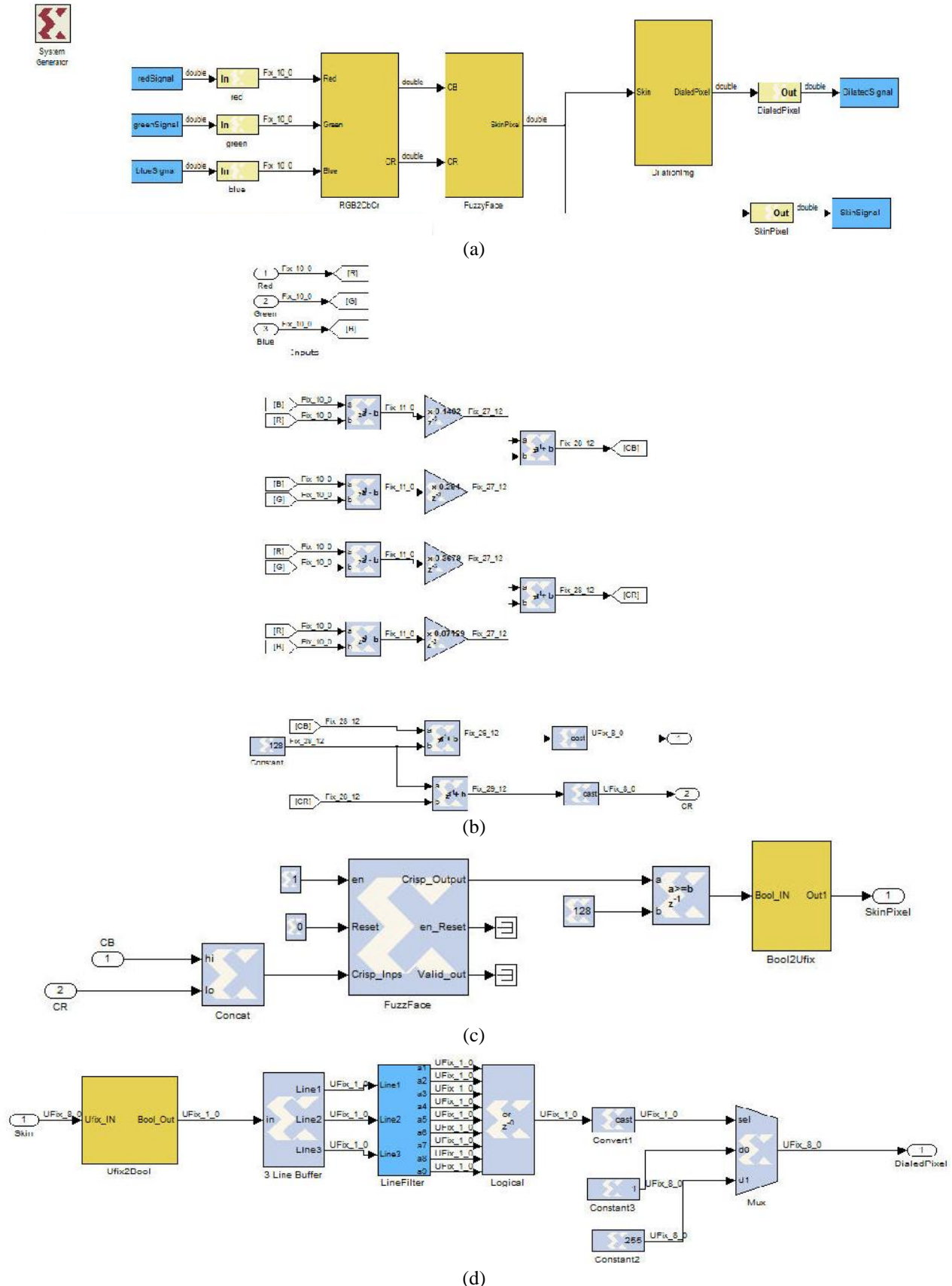

(a)

(b)

(c)

(d)

Fig.6: Top Level Module of Face Detection Algorithm in Xilinx System Generator.
(a) Complete Blocksets. (b) RGB2YCbCr Conversion Block.
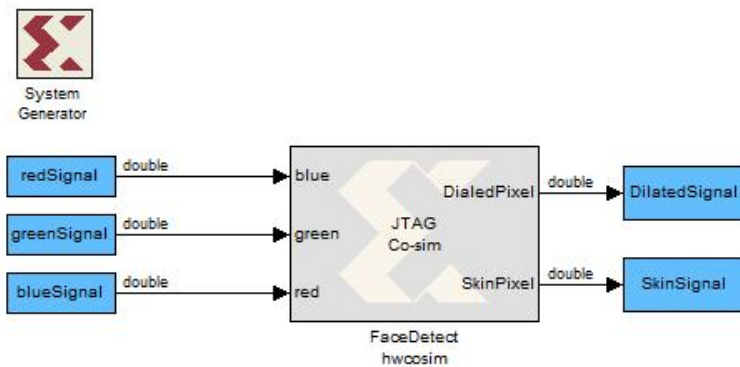(c) Fuzzy Face Block. (d) Dilated Image Block.

Fig.7: System Generator Project for Hardware-in-the-loop testing

And Fig.8 shows the skin image and the image after dilation for the input image.

B. Real-Time Face Detection

After the implementation of the face detection has completed, the next main objective is to develop a real-time face detection system where the input comes from a live video acquired from a CMOS camera and the detected edges to be displayed on a DVI display screen.

The setup for implementation consists of Video Starter Kit (VSK) consisting of Spartan 3A DSP XCSD3400A FPGA connected to a Micron CMOS camera of resolution 720 x 480 pixels delivering frames at 60 fps through a FPGA Mezzanine Card (FMC) Daughter card used for decoding the data arriving through the serial LVDS camera interface. The de-serialized input consists of V-Sync, H-Sync and 8 line data bus which serves as the input for the face detection model. The face algorithm is applied in the Camera Processing block on the input signal arriving from the Camera In block. The output signal is Gamma corrected for the output DVI monitor and is driven by Display controller to the DVI output monitor. Video to VFBC and MPMC core helps us to store the image data and buffer them to the output screen.

The status reporting and controlling of these blocks are carried out by Micro Blaze processor through Processor Local Bus (PLB). The block diagram of the setup is shown in Fig. 9. Xilinx provides a demo system with its System Generator software, named ""vsk_camera_vop.mdl" that accepts the camera input and processes the data with subsystems to control brightness, contrast, and other parameters. The concept for integration of the face detection algorithm was to create a new subsystem in this model, titled "FuzzFace Detection". Figure 10 shows the original system with the FuzzFaceDetection subsystem added. And the result face

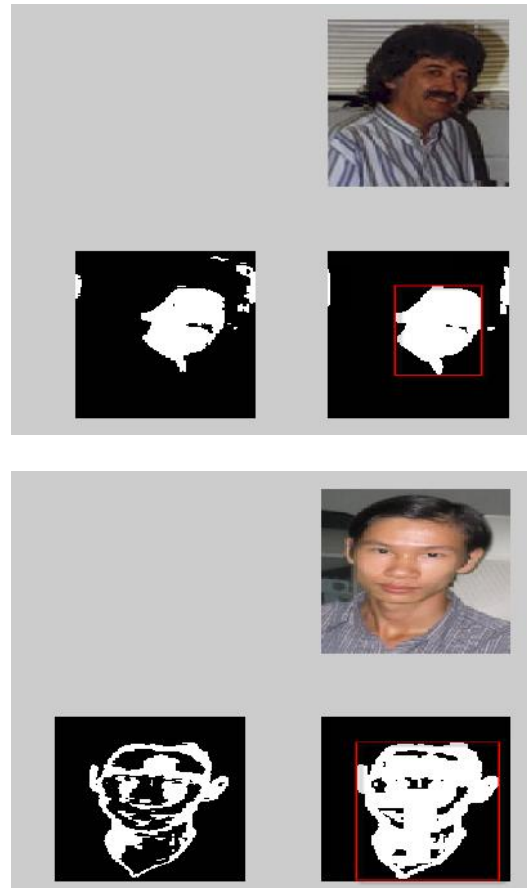detection image and dilated image of the real-time frame is shown in Fig.11.

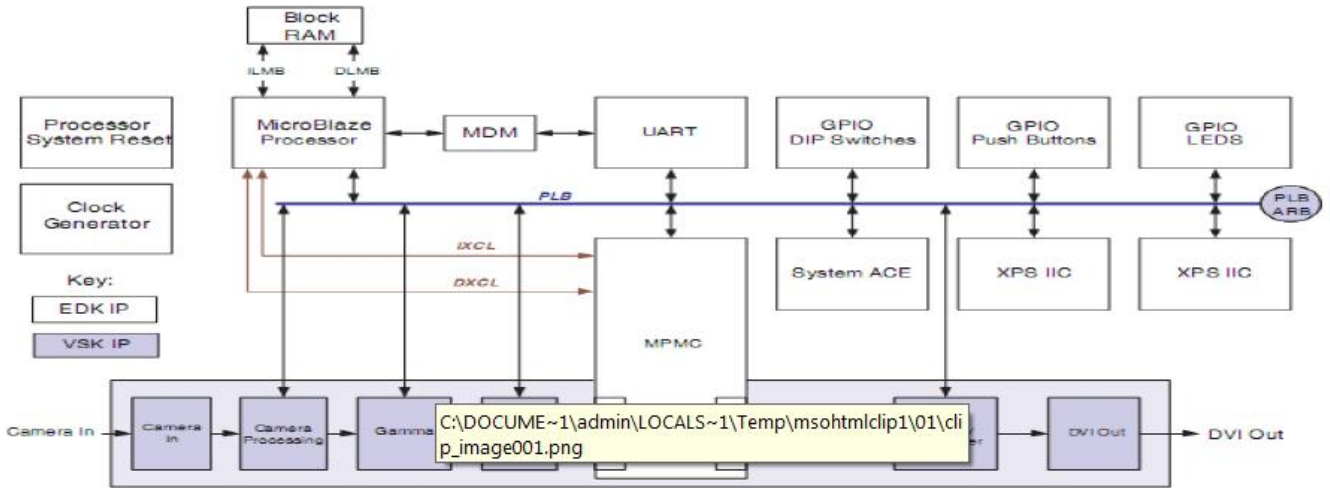Fig.8: Implementation of Still image Face Detection algorithm.

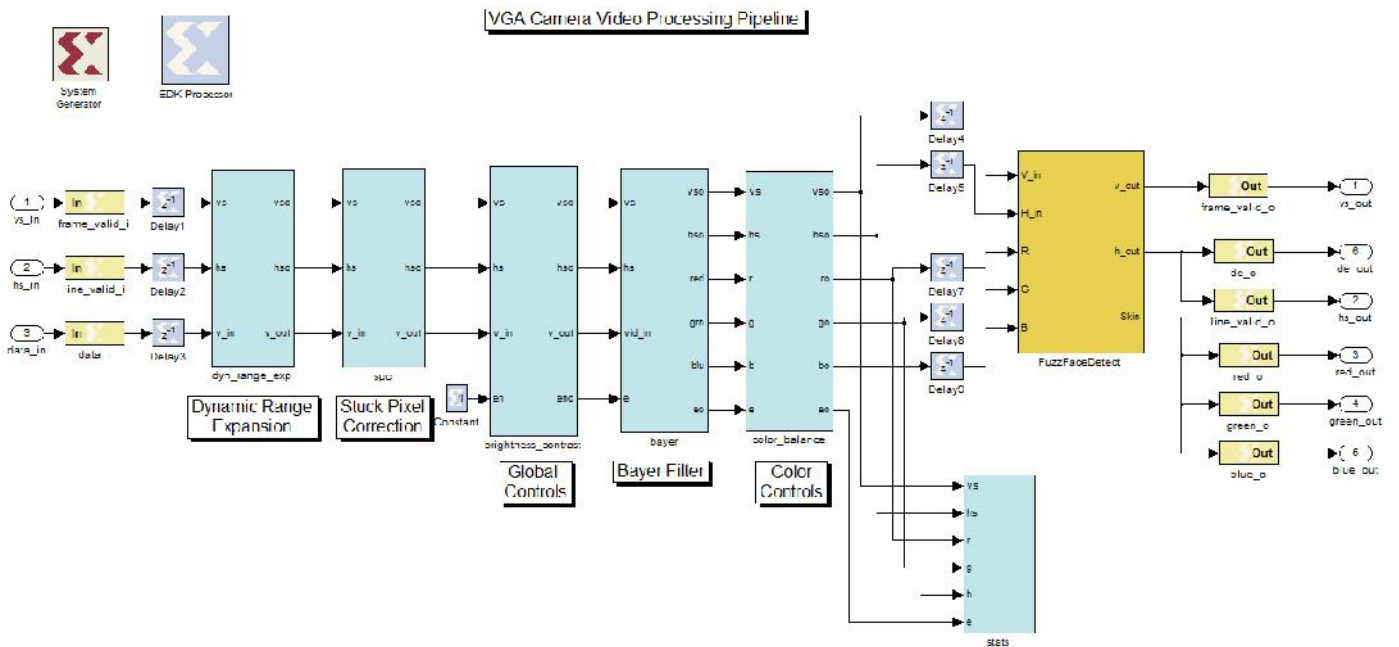Fig.9: Block Diagram of the Complete Setup

Fig.10: Top-Level Video Processing System
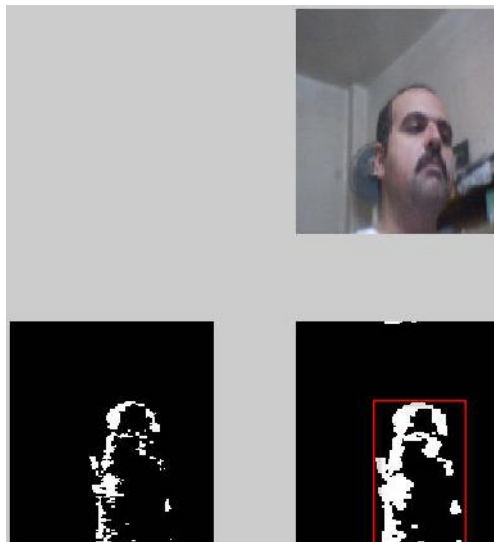

Fig.11: the result of real-time face detection implementation

5. CONCLUSION

This paper presents a novel and fast hardware architecture for face detection based on fuzzy rule based system using a fast FPGA-based general purpose fuzzy processor. The proposed fuzzy system models the skin color distribution in YCbCr color space. The parallel processing which FPGA is described is used to accelerate the processing speed of the face detection system. The proposed architecture for face detection has been designed using VHDL language and Xilinx System generator in MATLAB and implemented by XtremeDSP Video Starter kit – Spartan 3A Development Kit. Experimental results demonstrate that our system has achieved high detection rates and low false positives over a wide range of facial variations in color, position and varying lighting conditions in both still image and real-time system.

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