Signal Conditioner Circuit for Water Quality Monitoring Device using Current Differential Trans conductance Amplifier

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ABSTRACT

A new configuration realizing water quality monitoring device using photo catalytic sensor for the determination of chemical oxygen demand (COD) involving CMOS current differencing trans conductance amplifier (CDTA) based low pass filter free from trans conductance variation is proposed. The circuit uses four CDTA’s as active elements and together with two capacitors and one resistors as passive elements. The use of this active component makes the implementation simple and attractive. The functionality of the circuit is tested using Tanner simulator version 15 for a 70nm CMOS process model also the transfer function realization is done on MATLAB, the Very high speed integrated circuit Hardware description language (VHDL) code for the same scheme is simulated on Xilinx ISE and various simulation results are obtained. Simulation results are included to demonstrate the results.

Keywords: Chemical Oxygen Demand, Low Pass filter, CMOS, CDTA, Xilinx

1. INTRODUCTION

Monitoring the pH of water resources and sewage system for water pollution is typical and necessary task in today’s overdeveloped scenario. Now a day’s we have Semiconductor based micro sensors which are easily available and economical and able to react with the ion concentration, in other words activity of the ions. A photo catalytic sensor for the determination of chemical oxygen demand (COD) with flow injection analysis (FIA) based on the photo catalysis of organic compounds in the presence of titanium dioxide (TiO2) beads in a photochemical column is used to measure the quantity of COD. The sensor was developed in conjunction with TiO2 beads in the photochemical column and with an oxygen electrode as the sensing part. The sensor signal was observed as a result of the detection of dissolved oxygen changes due to photo catalytic oxidation of organic compounds in the sample solution. This sensor responded linearly to the CODmn of artificially treated wastewater (AWW) in the range of 0.12–8 ppm [1-3]. Photo catalytic sensor has been found several drawbacks related to thermal dependency, long-term drift, linearity, dynamic range. To improve the accuracy in the biomedical applications, it is necessary to find the compensation method to make the applications free from these effects. In order to capture the output response of the photo catalytic sensor, a readout interface is necessary. In this paper a new readout interface circuit having greater linearity, low power consumption, large bandwidth, by using current mode circuits (CMC’s) is proposed.

Conventional water quality monitoring applications are made up of voltage mode circuits (VMC) based on op-amps and OTA’s [3-5]. These applications are suffer from low band widths (BW’s) arising due to stray and circuit capacitances. Also the need for low voltage, low power circuits makes these circuits not suitable for water quality monitoring as these circuits required the minimum bias voltage depends on the threshold voltage of the MOSFET’s. However, with the advancement in the analog VLSI new analog devices are based on currents are developed called current mode circuits (CMC’s). These circuits have a significant advantage of low power, low voltages and can operate over wide dynamic range. These circuits, CMC can offer to the designer large bandwidths, greater linearity, wider dynamic range, simple circuitry and low power consumption. Current feedback op-amps (CFOAs), operational floating conveyors (OFCs) and current conveyors (CCs) etc. are popular CMC configuration and most widely used structure among them is CDTA, extension of the second-generation current conveyor (CCII). Hence, we decided to use the CDTA in the proposed scheme.

2. SEMICONDUCTOR PHOTO CATALYSIS

Explaining the aim of semiconductor photo catalysis is to effectively detoxify toxious organic pollutants. UV or visible light is used to create electron/hole pairs in semiconductor. The electron then react with oxygen in the sample to form O2- and hole reacts with surface hydroxyl groups to form OH radicals. The radical species then attack the organic molecule which is eventually oxidized to CO2 and H2O. It will produce HCL if the organic molecule contains chlorine.

Photo catalysis is an efficient method for the degradation and mineralization of organic compounds [6-8]. It has been the subject of numerous studies to obtain a better understanding of the mechanisms of the reactions involved [10]. A semiconductor particle is believed to have a filled valence band separated from a vacant conduction band by a gap whose energy is Eg. When irradiated with a light source, whose energy exceeds Eg, an electron is promoted from the valence to the conduction band, leaving behind a positive hole. Upon migration to the surface, the electron would reduce any available species. In contrast, when the hole reaches the surface, it would react with water to produce hydroxyl radicals. These
radicals play an important role in oxidizing organic pollutants. Molecular oxygen dissolved is also an essential component because it acts as scavenger of the photo generated electrons, forming a superoxide radical ion, and further reacting with transient radicals leading toward CO2 formation [11-14]. It was found that photo catalytic activity is almost completely suppressed in the absence of oxygen and the concentration of oxygen has a profound effect on the rate of photo catalyzed decomposition of organic compounds. Many of photo catalytic processes apply the TiO2 as a photo catalyst because it is non-photo corrosive, non-toxic, and capable of the photo oxidative destruction of most organic pollutants [15-17]. It is well known that the TiO2 photo catalysis leads to stoichiometric photo mineralization of organic compounds.

3. CDTA

In Since an introduction of the current differencing trans conductance amplifier (CDTA) in 2003, it has been acknowledged to be a versatile current-mode active building block in designing analog circuits [18]. This device that has two current inputs and two kinds of current output provides an easy implementation of current-mode active filters [19]. It also exhibits the ability of electronic tuning by the help of its trans conductance gain (gm). All these advantages together with its current-mode operation nature make the CDTA a promising choice for realizing the current-mode filters. As a result, a variety of CDTA applications has also been considered by various researchers [20-23].

4. CMOS realization of CDTA

The circuit representation and the equivalent circuit of the CDTA are shown in Fig.2. The terminal relation of the CDTA can be characterized by the following set of equations (1-3).

\[
\begin{align*}
I_z &= 0 \quad 0 \quad 0 \quad (-1)I_w \\
V_w &= 1 \quad 0 \quad 0 \\
I_x &= g_m \quad 0 \quad 0 \\
V_p &= 0 \quad 0 \quad 0 \quad (1)
\end{align*}
\]

where p and n are input terminals, z and ±x are output terminals, gm is the trans conductance gain, and Zz is an external impedance connected at the terminal z.

According to above equation and an equivalent circuit of Fig.2(b), the current flowing out of the terminal z (iz) is a difference between the currents through the terminals p and n (ip-in). The voltage drop at the terminal z is transferred to a current at the terminal x (ix) by a trans conductance gain (gm),
which is electronically controllable by an external bias current (IO). These currents, which are copied to a general number of output current terminals x, are equal in magnitude but flow in opposite directions. Although there are several techniques to realize the CDTA, one possible bipolar realization is shown in Fig. 3 [24-25]. It mainly comprises a current differencing circuit formed by two current followers Q1-Q9, a basic current mirror Q10-Q11, and a multiple-output trans conductance amplifier Q12-Q42. In this case, the trans conductance gain $g_m$ of the CDTA is directly proportional to the external bias current IO, which can be written by

$$g_m = \frac{I_B}{2V_T}$$  \hspace{1cm} (4)

where $V_T = 26 \text{ mV}$ at $27^\circ \text{C}$ is the thermal voltage.

5. Device Description and Mathematical Modeling

The block diagram of the proposed scheme is shown below it consists of one CDTA, two capacitors, one resistors, photo catalytic sensor, Current Mirror. One of the drawbacks of the Current conveyor device is that its trans conductance ($g_m$) varies often with the $I_{bias}$. To make the device free from trans conductance variation we used current mirrors along with the current conveyors which are capable of providing the constant $I_{bias}$ and thereby, making the device free from change of trans conductance effect. Various kinds of Current mirrors are found but, to make the design low power PMOS bulk-driven cascade current mirror is used. The topology of the low-voltage PMOS bulk-driven cascade current mirror is used to control the $g_m$ of the CDTA.

The transfer function of the proposed scheme is calculated as below

$$I_o = \frac{b_0s^2 + (b_0 + a)s}{D(s)}$$  \hspace{1cm} (5)
\[ D(S) = S^2 + b_1 S + b_0 \] (6)

Where \( b_0 = \frac{g_m}{R C_2}, b_1 = \frac{1}{R C_1} \), \( a = \frac{g_m}{C_2} \)

From (6) \( \omega_0 \) and \( Q \) of the proposed circuit is given as

\[ \omega_0 = \frac{g_m}{R C_2} \] (Natural frequency)

\[ Q = \sqrt{\frac{g_m R C_1 C_2}{C_2}} \] (Quality factor)

\[ B = \frac{\omega_0}{Q} \] (Bandwidth)

Take the typical values of Passive elements \( R = R_1 = R_2 = 1 \text{k}\Omega \), \( C_1 = C_2 = 20\text{pF} \) \( g_m = 800\mu\text{s} \) we get,

For optimization take \( I_{12} = 0 \)

\[ I_{LP} = \frac{2b_0}{D(S)} = 2 \times 10^{15} \]

\[ b_0 = \frac{g_m}{R C_2} = 2 \times 10^{15} \]

\[ I_{LP} = \frac{2b_0}{D(S)} = \frac{2 \times 10^{15}}{S^2 + 5 \times 10^{-7}S + 2 \times 10^{15}} \]

The nyquist and Bode plot of the above transfer function is plotted with the help of MATLAB.

Figure 6-7 shown above justify that the transfer function of the system is closed loop stable with phase margin of 68.5 degree at frequency 3.5 MHz.

6. Current Mirror

One of the drawbacks of the Current conveyor device is that its trans conductance \( (g_m) \) varies often with the \( I_{bias} \). To make the device free from trans conductance variation we used current mirrors along with the current conveyors which are capable of providing the constant \( I_{bias} \) and thereby, making the device free from change of trans conductance effect.

To make the design low power PMOS bulk-driven cascade current mirror (PMOS BDCCM) is used. The topology of the low-voltage PMOS bulk-driven cascade current mirror is shown in Figure 8.

Minimum input output voltage drops may be described as

\[ V_{dd} - V_{in} \text{ (min, BD)} = V_{SD1} + V_{SD2} \]
\[ V_{dd} - V_{out} \text{ (min, BD)} = V_{SD3} + V_{SD4} \]
\[ V_{dd} - V_{in} \text{ (min, GD)} = V_{SG} = V_{TD} + \text{VT} \]
\[ V_{dd} - V_{out} \text{ (min, GD)} = 2V_{SD, \text{sat}} \]

The input voltage drop of BDCCM is

\[ V_{dd} - V_{in} \text{ (min, GD)} = V_{SB1} \leq 0.3 \text{ V} \]

This is much lower than GDCCM.

Fig.7 nyquist plot of the above transfer function

Fig.6 bode plot of the above transfer function

Fig.8 PMOS bulk-driven cascade current mirror
Consequently M1 and M2 are forced to work in linear region
VSG1 > VSG2
ISD1 = ISD2
forcing \( \frac{W_2}{L_2} > \frac{W_1}{L_1} \)
VSB => VDD-VSD1-Vb\( \leq 0.3 \)
Hence Vb \( \geq VDD - VSD1 - 0.3 \)
for VSB1 = VSB3 and VSG1 = VSG3 then ISD1 = ISD3
If M3 also were in linear region VSD1 = VSD4

Since the source drain voltage of M4 is unrestricted M4 may
work in linear or saturation region obviously minimum output
voltage drop BDCCM is lower than GDCCM. The bulk-driven
technique may eliminate the limitation of the threshold voltage
on the signal channel effectively, thereby reducing the supply
voltage required by CMOS analog IC. Compared with the
normal gate-driven CMs, the low-voltage BDCCM reduces the
input/output voltage drop greatly and has a good input/output
resistance characteristic along with a better current driving
ability.

7. SIMULATION AND RESULTS ANALYSIS

Simulation of a readout interface circuit for water quality
monitoring device using photo catalytic sensor involving
second generation current conveyors have been carried out on
Tanner simulator version 15 for a 70nm CMOS process model.
In the proposed circuit, following typical values for passive
components were chosen Figure 9: R9 = 1kΩ, C1 = C2 = 20pF
gm = 800μs. The proposed readout circuit is modeled
using Tanner Tool Version 15 in 70nm technology and shown in
Figure 8. The output response of the device with respect to the
time i.e transient analysis shown in Figure 9 justify the device
is highly linear. The power results obtained when the device is
simulated 70nm technology is shown in the appendix at the end
of the paper and it is found that the device consumes the average
power of 4.531175e-002 watts. The device is found stable as
shown in the mathematical modeling by the analysis of the
transfer function and by bode and nyquist plot.

8. Conclusion

In this paper, a new interface readout circuit employing CMOS
current differencing trans conductance amplifier (CDTA) is
proposed. The second-generation current conveyor introduced
is a convenient building block that provides a simplified
approach to the design of linear analog systems. The bulk-
driven technique used to control the trans conductance effect
of CDTA may eliminate the limitation of the threshold voltage,
thereby reducing the supply voltage required by CMOS analog
IC. Results of computer simulations and the comparison with
experimental data and with transistor-level simulation
demonstrated an accuracy of the approach. All the results are in
good agreement with the theoretical analysis. This study may
be extended and more improvement in terms of power and size
can be achieved at layout level and thus more effective results
may be obtained.
REFERENCES


Appendix
Simulation results
Release 10.1 - xst K.31 (nt)
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--> Parameter TMPDIR set to C:/Documents and Settings/BPT/MMCCdevice/device/ccdevice/c dta/opt/trr/xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs

--> Parameter xsthdppdir set to C:/Documents and Settings/BPT/MMCCdevice/device/ccdevice/c dta/opt/trr/xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.22 secs
--- Reading design: Cell1.prj

--* Synthesis Options Summary*--

- **RTL Output**: Yes
- **Global Optimization**: Yes
- **All Clock Nets**: Yes
- **Read Cores**: Yes
- **Write Timing Constraints**: No
- **Cross Clock Analysis**: No
- **Hierarchy Separator**: /
- **Bus Delimiter**: <>
- **Case Specifier**: maintain
- **Slice Utilization Ratio**: 100
- **BRAM Utilization Ratio**: 100
- **Verilog 2001**: Yes
- **Auto BRAM Packing**: No
- **Slicé Utilization Ratio Delta**: 5

--- Source Parameters

- **Input File Name**: "Cell1.prj"
- **Input Format**: mixed
- **Ignore Synthesis Constraint File**: NO

--- Target Parameters

- **Output File Name**: "Cell1"
- **Output Format**: NC
- **Target Device**: xc3s100e-5-vq100

--- Source Options

- **Top Module Name**: Cell1
- **Automatic FSM Extraction**: Yes
- **Safe Implementation**: No
- **FSM Style**: lut
- **RAM Extraction**: Yes
- **RAM Style**: Auto
- **ROM Extraction**: Yes
- **Mux Style**: Auto
- **Decoder Extraction**: YES
- **Priority Encoder Extraction**: NO
- **Shift Register Extraction**: YES
- **Logical Shifter Extraction**: YES
- **XOR Collapsing**: YES
- **ROM Style**: Auto
- **Mux Extraction**: YES
- **Resource Sharing**: YES
- **Asynchronous To Synchronous**: NO
- **Multiplier Style**: auto
- **Automatic Register Balancing**: NO

--- Target Options

- **Add IO Buffers**: Yes
- **Global Maximum Fanout**: 500
- **Add Generic Clock Buffer(BUFG)**: 24
- **Register Duplication**: YES
- **Slice Packing**: YES
- **Optimize Instantiated Primitives**: NO
- **Use Clock Enable**: Yes
- **Use Synchronous Set**: Yes
- **Use Synchronous Reset**: Yes
- **Pack IO Registers into IOBs**: auto
- **Equivalent register Removal**: YES

--- General Options

- **Optimization Goal**: Speed
- **Optimization Effort**: 1
- **Library Search Order**: Cell1.lso
- **Keep Hierarchy**: NO
- **Netlist Hierarchy**: as_optimized

--- Power result

* Device and node counts:
  * MOSFETs - 20  MOSFET geometries - 4
  * BJTs - 0  JFETS - 0
  * MESFETS - 0  Diodes - 0
  * Capacitors - 0  Resistors - 0
  * Inductors - 0  Mutual inductors - 0
  * Transmission lines - 0  Coupled transmission lines - 0
  * Voltage sources - 5  Current sources - 2
  * VCVS - 0  VCCS - 0
  * CCVS - 0  CCCS - 0
  * V-control switch - 0  I-control switch - 0
  * Macro devices - 0  External C model instances - 0
  * HDL devices - 0
  * Subcircuits - 0  Subcircuit instaces - 0
  * Independent nodes - 12  Boundary nodes - 6
  * Total nodes - 18

*SEDIT: Analysis types DCOP 0 ACMODEL 0 AC 0 TRANSIENT 1 TRANSFER 0 NOISE 0

*WEDIT: .tran 2e-009 5e-009

**TRANSIENT ANALYSIS**

```plaintext
Time>s>  v(in)<V>  v(out)<V>
0.000000e+000  0.000000e+000  1.1508e+000
1.250000e-010  1.250000e-001  1.1550e+000
1.375000e-009  1.375000e+000  1.1983e+000
2.926462e-009  2.9265e+000  1.2525e+000
4.578586e-009  4.5786e+000  1.3102e+000
5.000000e-009  5.000000e+000  1.3253e+000
```

*BEGIN NON-GRAphICAL DATA*

**Power Results**

- **vd from time 0 to 5e-007**
  - Average power consumed - > 4.531175e-002 watts
  - Max power 6.167927e-002 at time 3.05e-007
  - Min power 3.455305e-002 at time 5e-009

* END NON-GRAphICAL DATA

* Parsing 0.01 seconds
* Setup 0.00 seconds
AUTHOR PROFILES

Dr. Pawan Whig did B.Tech in Electronics and Communication Engineering in 2005 and completed M.Tech in VLSI in 2008. He has a Ph. D. degree from Jamia Milia Islamia. He has been working in the field of Electronics and Communication from last 15 years. Before joining Vivekananda Institute of Professional Studies, was working as Dean Academics and Professor in E&C Department at RIET Jaipur. He is reviewer of several internationals refereed journals. He has been designing and mentoring several projects in universities across India. He is member of International Association of Engineers Hong Kong, ISTE, IEEE, SCI, IEI and state student coordinator of Rajasthan of Computer Society of India (CSI). He has published technical articles in more than 50 nationals and internationals journals. He has wide area of research like Analog Signal Processing, Sensor Modeling, Water Quality Monitoring Applications and Simulation & Design. He has invented a Low Power Water Quality Monitoring Device which is under Patent Process. He has proposed a SPICE Model for Novel Photo catalytic Sensor (PCS) which can be the area of interest for new researcher in the same field.

Dr. Syed Naseem Ahmad is currently working as a Head of Department (ECE) in Jamia Milia Islamia University Jamia Nagar India; New Delhi - 110025. He did bachelor in electrical engineering in 1975 from Aligarh Muslim University. He did his M.Tech degree from the same university in Instrumentation and Control engineering in 1978. He has done PhD from JMI. He has wide area of research ranging from Analog Signal Processing, Image processing and communication engineering. He has guided many research fellows. He has worked as a reviewer for several conferences and Journals both national and international. He is author of more than 50 scientific contributions including articles in international refereed Journals and Conferences.