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Design and Analysis of AWG and Re-Circulating Buffer based Optical Packet Switch

[1] Bharat Mishra, [2]Anjaney Nigam, [2]Prabhat Patel
[1] Department of Information Technology in Mahatma Gandhi Chitrakoot Gramodaya University Chitrakoot Satna, Madhya Pradesh, India
[2] Department of Electronics and Telecommunication, Jabalpur Engineering College, Jabalpur, Madhya Pradesh, India
E-mail: [1] bharat.mgcgv@gmail.com, [2] anjaneyknp@gmail.com, [3] ppatel@jecjabalpur.ac.in

ABSTRACT

Optical switches are essential not only in optical packet networks but also in data centers. This paper, discusses a optical packet switch design. The switch design considered in the paper is re-circulating in nature. The re-circulating nature is achieved with a few components in compare to earlier switches design published in past. This paper presents a mathematical framework, to obtain number of re-circulation count of the packet inside the buffer. Thus required amount of power for correct operation of switch is lesser in comparison to earlier designs.

Keywords: *AWG, TWC, re-circulating buffer*

1. INTRODUCTION

Optical communication offers very high speed data transfer, over a long distance with very little distortion. Over the past few years optical communication is an integral part of backbone optical networks. In recent past use of optics in data centers (DC) is investigated and it has been found that optical Top of Rack (TOR) switches will be integral part of the DC. However, the required number of switches in DC is some hundreds or thousands in comparison to tens of switches in optical networks. Therefore, the design of optical switches is very important, and switch with low loss, less energy hungry, lesser crosstalk is desirable. In view of these parameters Arrayed Waveguide Gratings (AWGs) based optical switches has emerged and many optical switch designs are proposed. First notable AWG based design was proposed Srivastva et al., where routing pattern of AWG was used very efficiently along with very simple buffer design for the storage of contending packets. As in FDL buffer storage duration is limited, use of electronic buffer based design is proposed in [1]. However, extra cost in terms of O/E and E/O is to be paid. Recently, buffer less AWG based design is proposed, where automatic re-transmission of blocked/dropped packets is proposed. However, due to buffer less design numbers of dropped packets are very large, thus in turn more re-transmission of contending packets. Other AWG based notable projects are LIONS [2], IRIS [1], PROTEUS [3] and Petabit [4] etc.. However, when Quality of Services (QoS) are included in arriving data like priority then low priority packets may stay in the buffer for longer duration. Therefore, re-circulating buffer is essential for longer duration storage. In past, various re-circulating buffer type optical switch designs are proposed, where buffering capacity of eight is easily achieved with required power in milii-watts. This paper explores the recently proposed switch design in terms of power requirements which is required for longer duration storage.

2. RELATED WORKS

This section discusses some recently published optical packet switched architectures with their pros and cons.

A. Re-circulating loop buffer type broadcast and select switch

The first notable re-circulating type buffer design was proposed by Bendali [5]. The architecture proposed by R. Srivastava is similar to the architecture proposed by Bendali, but with lots of advantages [6-8]. The architecture consists of *N* Tunable Wavelength Convertor s one at the input, a re-circulating loop buffer is used for storing the contending packets and *N* fixed filters one at each output. In the design further modification were suggested to further reduce the physical loss of the switch by replacing splitter and tunable filter (TF) combinations with AWG demux and fixed filters (FF) .

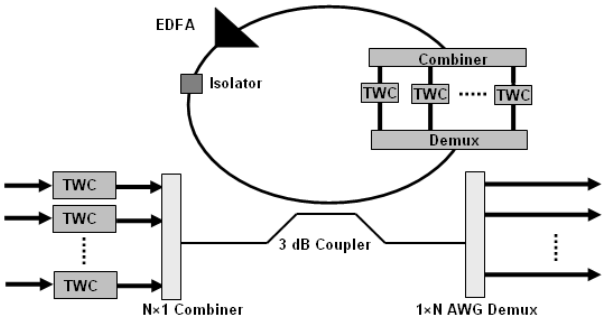

Fig. 1: Re-circulating loop buffer type broadcast and select switch

In both architectures (R. Srivastava 2003 and Bendelli 1995), incoming packets used WDM technology to share common piece of fiber. The size of the buffer (buffer wavelengths) depends on the packet loss probability, desired traffic throughput and various component parameters. Packets are transferred in the buffer by tuning their wavelengths appropriately which are passed by buffer demux and blocked

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by output demux. Thus packets keep on circulating till contention resolve. For reading out of the packet from the buffer, the corresponding TWC will tune the wavelength of the packet such that it is passed by output demux and received by particular filter only. It is noticeable that the buffer and output demux wavelengths are disjoint.

The placement of the TWC inside the buffer can reduce the packet loss probability [9]. Because the implication of the TWC inside the buffer can also resolve contention in the wavelength domain as well as simultaneous read/write operation is possible in single time slot. The packets to be buffered are converted to the free wavelengths available in the buffer; if memory is full (all the wavelengths have already been allocated) then packet cannot be stored and considered as lost.

B. TFBGs Based Optical Switch (*TFBGOS*)

In the above design, physical losses occurred in the buffer is huge, thus storage lime is limited or in other words the number of allowed re-circulation is very limited even a power level of mili-watts [10].

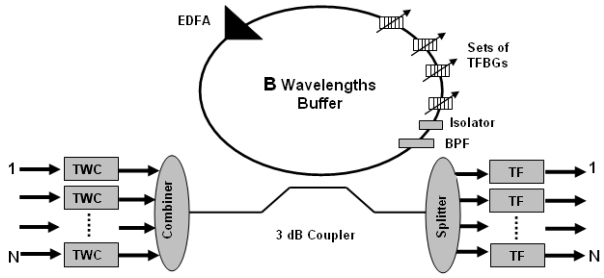

Fig. 2: Design of TFBG based Switch

In nut-shelll the major problems of the loop buffer based architectures are,

1) Large physical loss

2) Separate control is required for each packet, therefore Demux/Mux, SOAs/TWCs are required in the buffer.

3) Scaling in-efficient

4) Circulation limits

5) More numbers of required components.

In this architecture Demux and combiners (lossy device) are not required. This simplification reduces the physical loss of the switch. Therefore, circulation limit is relaxed, and full buffer capacity can be utilized effectively. Apart from this, for the controlling of packets inside the buffer, no separations are required.

The architecture is designed for equal length packets, and these packets are assumed to be aligned in timing, when they arrive at the switch input. This synchronization is necessary for the correct switch operation, and can be achieved using the techniques defined in the literature [11]. The synchronization between TFBG and TF can be achieved by output synchronization scheme. Thus synchronization is assumed at both input and output of the switch. In the loop buffer, automatic gain control (AGC) scheme is also assumed, which keeps the gain of the EDFA constant irrespective of the numbers of channels passing through it [12].

In both these designs, buffer is re-circulating in nature, but due to the large numbers of required devices power required for correct operations of the switch is in mili and sub mili watts region.

3. ARCHITECTURE DESCRIPTIONS

The figure 3, shows an AWG based optical packet switch architecture proposed by H. Rastegarfar [13]. This architecture is single wavelength re-circulating architecture which uses fiber delay lines of unit slot for storing the contended packets. In this design when situation of contention among packets arise then packets are forwarded towards re-circulating ports (1 to 8, refer Figure 1) and when contention among packets resolve, packets can be read out from the buffer by tuning their wavelengths and dispatching them towards the appropriate output ports.

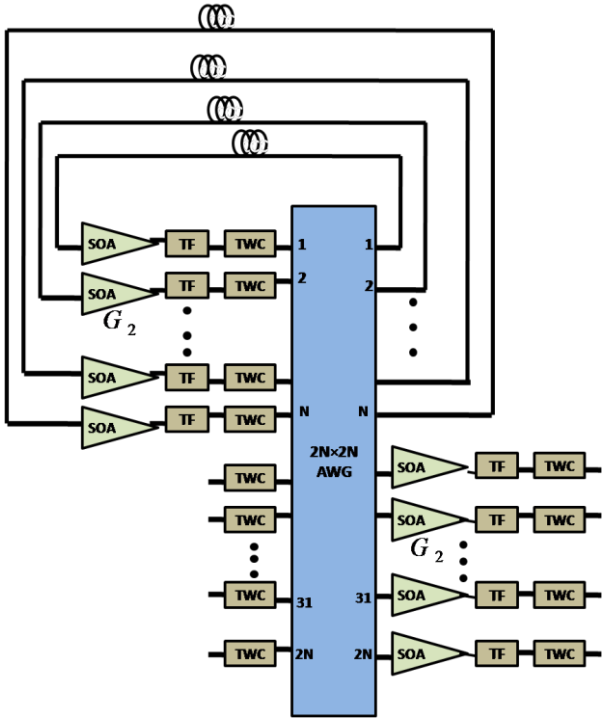

Fig.3: Layout of AWG based switch A1 (H. Rastegarfar)

This architecture is the modified version of the architecture presented in [14], with the difference that in this design buffer is re-circulating in nature. Such type of buffers are required when QoS parameters like priority is set for the packets. In case of prioritized traffic, high priority packets given preference over lower priority packets, thus a situation may arise when low priority packets may remain in the buffer for longer duration.

The FDLs are of unit slot durations. The loss suffered by the packet inside the buffer is due to AWG, TF and TWC is compensated by SOAs placed in each FDL. However, the physical loss of the device is lesser in comparison to earlier re-circulating type design as the required numbers of components are very lesser in number.

4. ANALYSIS OF THE SWITCH

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This section presents the analysis of the switch in terms of power and noises and bit error rate (BER).

A. Power and Noise Analysis

Power received at the output of the switch is

$$P_{out} = bP_{in}L_{in} + n_{sp}(G_2 - 1)h\nu B_o \sum_{i=1}^{K}(L_b G_2)^i + (G_2 - 1)h\nu B_o L_{out} G_2 \quad (1)$$

Where,

$$L_{in} = L_{TWC}L_{AWG} \quad (2)$$

$$L_b = L_{TWC}L_{AWG}L_{SOA}L_{TF} \quad (3)$$

$$L_{out} = L_{TWC}L_{TF}L_{SOA} \quad (4)$$

b=0,1 for bit '0' and '1' respectively (5)

The description of the parameters used in various eqn. is described in Table 1.

Loss of the loop and output unit is fully compensated by the gain of SOA, i.e., $L_b G_2 = 1$ and $L_{out} G_2 = 1$ then

$$P_{out} = P_{in}L_{in} + n_{sp}(G_2 - 1)h\nu B_o(K+1) \quad (6)$$

Due to square law detection by the photo detector in the receiver, various noise components are generated. These noise components are shot noise, ASE-ASE beat noise, sig-ASE beat noise, shot-ASE beat noise and thermal noise variances are denoted by σ_s^2, σ_{sp-sp}^2, σ_{sig-sp}^2, σ_{s-sp}^2, and σ_{th}^2 respectively [13]. For bit b the different noise components in the receiver are:

$$\sigma_s^2 = 2qRPB_e$$

$$\sigma_{sp-sp}^2 = 2R^2P_{sp}(2B_o - B_e)\frac{B_e}{B_0^2}$$

$$\sigma_{sig-sp}^2 = 4R^2P\frac{P_{sp}B_e}{B_0}$$

$$\sigma_{s-sp}^2 = 2qRP_{sp}B_e$$

$$\sigma_{th}^2 = \frac{4K_BTB_e}{R_L} \quad (7)$$

The total noise variance for bit *b* is

$$\sigma^2(b) = \sigma_s^2 + \sigma_{sp-sp}^2 + \sigma_{sp-sig}^2 + \sigma_{s-sp}^2 + \sigma_{th}^2 \quad (8)$$

$$BER = Q\left(\frac{I(1) - I(0)}{\sigma(1) + \sigma(0)}\right) \quad (9)$$

$$Q(z) = \frac{1}{\sqrt{2\pi}}\int_z^{\infty} e^{-\frac{z^2}{2}}dz \quad (10)$$

Where I (1) $=RP$ (1) and I (0) $=RP$ (0) are photocurrent sampled by receiver during bit 1 and bit 0 respectively, and R is responsivity of the receiver.

B. Calculation

Using the above formulation and the values of the parameters as given in Table 1, the results obtained in terms of maximum number of allowed re-circulations at different power levels for fixed BER≤10^{-9} is presented in Table 2. In the simulation a 16×16 AWG switch is considered, the ports 1 to 8 are used as actual inputs and outputs, while other ports 9-16 are used for buffer creation. To utilize full buffer capacity of 8, 2µW power is required, which is very lesser in comparison to earlier proposed designs [8]

Table 1. List of Parameters and their Value. [15]

Parameters	Value
Size of the switch	4
Population inversion factor	1.2
Speed of light	$3\times10^8 m/s$
Refractive index of fiber	1.55
Responsivity	1.28 A/W
Electronic charge	$1.6\times10^{-19}C$
Electrical bandwidth	10GHz
Optical bandwidth	20GHz
TWC insertion loss	2.0 dB
Loss of TF	2.0 dB
Loss of the fiber loop	0.2 dB/km
Loss of each FBG	1.0 dB
Loss of Circulator	1.0 dB

Table 2. Power vs. Allowed Re-circulations

Power (µW)	Allowed Re-circulations (BER≤10^{-9})
1	4
2	8
3	12
4	17
5	21
6	25
7	29
8	34
9	38
10	42

4. COMPARSION WITH RE-CIRCULATING TYPE BUFFER DESIGN

Table 3: Comparison of switch design

Reference	Power level
[15]	3 mW
[19]	100 µW
Proposed	2 µW

To fully utilize the buffer capacity a relatively very small power of 2 µW is requited which is very lesser in comparison to earlier designs.

5. CONCLUSIONS

Photonic packet switches can fulfill the demand for higher bandwidth. To increase throughput, switch architecture must utilize the buffer capacity fully. This has been found that switch can operate lower power level of micro-watts as compared to earlier design where power levels are in milli-watts.

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AUTHOR PROFILES

Dr. Bharat Mishra Dr. Bharat Mishra is an Associate Professor in Department of Information Technology in Mahatma Gandhi Chitrakoot Gramodaya University Chitrakoot satna (M.P.). He is having 25 year experience.

Mr. Anjaney Nigam Nigam is a Ph.D. research scholar in Mahatma Gandhi Chitrakoot Gramodaya University (MGCGU) Chitrakoot Satna(M.P.). He has six year teaching as an Assistant Professor in department of Electronics and Communication Engineering in Maharana Pratap Engineering college Kanpur. His main Area of interest is Optical Fiber Communication Technology and Microprocessors.

Dr. Prabhat Patel is an Associate Professor in Department of Electronics and Telecommunication, Jabalpur Engineering College, Jabalpur, Madhya Pradesh, India. He received Bachlor of Engineering degree in 1994 from Awadhesh Pratap Singh University, Rewa. He received his M. Tech.: 2001 (Communication Systems) from IIT, Kanpur and PhD: 2011 (Wireless Communication) from IIT, Kanpur. Currently he is also working as Reviewer of IEEE conference papers, and also the member of IEEE.

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