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Performance Evaluation of a New Eleven Level Transistor Clamped T-Type Multilevel Inverter

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ABSTRACT

Multilevel inverters (MLIs) are a type of converters that is fairly recent and uses power electronics switches. They are generally used to convert dc to ac power. Two-level inverters are regularly used to generate ac power; however, they require the switches to be operated at a relatively high switching frequency. Furthermore, with switches running under high dv/dt stress, the two-level inverter needs the employment of LC filters. The MLIs have the advantage of being able to generate a stepped ac waveform by combining many dc voltage sources with the right switch configuration. This paper presents a new eleven-level transistor clamped T-type multilevel inverter topology. The nearest level modulation (NLM) technique is used for the calculation of switching angles for a combination of appropriate switches. In comparison to a conventional multilevel inverter including cascaded H-bridge, Flying capacitor and Neutral point clamped topologies, this inverter requires far fewer semiconductor switches and isolated dc sources. In comparison to other traditional inverters with the same output quality, the suggested inverter provides superior output quality with lower power loss, according to the findings. MATLAB/Simulink simulation is carried out to verify the proposed topology, and the simulation results are discussed. From the result, the proposed eleven-level transistor clamped T-type inverter has lower total harmonic distortion.

Keywords: *New inverter, multilevel inverter, transistor clamped, T-type, 11 level, thd*

1. INTRODUCTION

In present era, Multi-Level Inverters (MLI) certainly gain huge importance owing to unique properties such as generating output voltage levels with minimum harmonics, a reduce burden on switching devices and fewer instances of electromagnetic interference Rodriguez, Lai and Peng [1], [2-4. A nearly sinusoidal waveform is achieved with a higher number of MLI levels. The THD in the ac output decreases as the number of MLI levels increases [5, 6]. By properly turning on and off the power switches, the modulation technique accomplishes its goal. Renewable energy applications, static reactive power compensators, and adjustable speed drives generally utilize multilevel inverters [7-9]. The inverters that generate only two levels at its output requires a switching frequency which is very high [3, 10, 11]. The existing conventional designs of MLI include Cascaded H-Bridge (CHB), Neutral Point Clamped (NPC) and Flying Capacitors (FCs) out of which CHB inverter feats minimum quantity of devices [7, 12-14]. It is also notable that diode-clamped inverter was designed by use of series bank of capacitors to generate alike voltage levels [7, 13, 15, 16]. The incorporation of differing magnitudes of DC sources allows the cascaded multi-level inverter topologies to be set into symmetric and asymmetric forms. With the same number of power electronic components, asymmetrical topologies can yield greater voltage levels [4, 17, 18]. A full bridge inverter is used in a variety of asymmetrical topologies to achieve negative voltage levels at the output [19]. This prompts the expanded intricacy of the general framework. The customary adjustment strategies can be custom-made to work with different staggered inverter designs. The regulation methods differ contingent upon the application that the design is utilized for and every procedure has its own merits and demerits. The various modulation techniques applied for cascade multi-level inverters are Level shift pulse width modulation (LS-PWM), Selective Harmonic Elimination (SHE), Multicarrier PWM, NLM and Hybrid modulation [20-22]. The topology reported in [23] investigation reflects the advancement of multi-level output voltage by altering the DC voltage sources either in series or parallel. It is also noticed that the merit of design in [24-26] lies in its credibility to generate five levels with a minimized component number in comparison with the conventional variations. The circuit requires five switches, one source, and two capacitors to generate five levels but it increases for more levels when connected in cascaded mode. Due to the substantially decreased number of switching devices and fewer dc sources required in the circuit design, the transistor clamped H-bridge (TCHB) multilevel inverter has recently attracted increased interest [24-26].

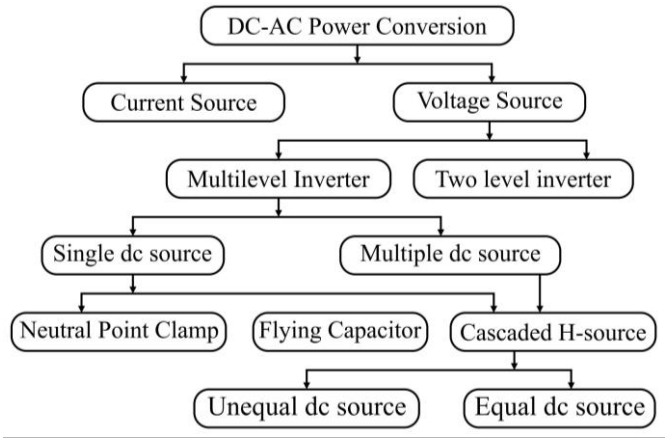

Figure 1. Classification of multilevel inverters [27]

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This paper suggests a transistor clamped T-Type asymmetrical inverter topology for medium voltage applications that is capable for creating eleven-levels (five-positive levels, five-negative levels and a zero-level) of the result voltage by using just nine switches. Another merit of proposed topology is that it achieves the level levels output by using only a combination of two DC sources. Some bidirectional switches are used that helps in the inversion of the current flowing through the connected load. A remarkable element of this topology is its ability of delivering negative levels without actually connecting an H-bridge before the load. A broad correlation of the proposed topology with recently proposed topology is listed out to signify precedency. The simulation results are furnished for resistive and inductive loads. The paper is organized in the following manner: Section II discusses the proposed inverter's configuration, Section III discusses NLM switching strategy, Section IV compares several conventional inverters and some of the recently proposed inverters, Section V discusses simulation verification, and Section VI concludes.

2. PROPOSED TOPOLOGY

Figure 2 illustrates the circuit of the proposed topology that contains of a DC voltage source within an H bridge with the switches S_6, S_7, S_8, and S_9. Furthermore, It shows two voltage sources (V_{dc1}, V_{dc2}), and total nine switches (S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8 , S_9). The switches S_6, S_7, S_8 and S_9 enables the power to get reversed at the load side. C_1 and C_2 are two capacitors connected at the input side and distributes equal magnitude of $V_{dc2}/2$ across each one of them. The proposed circuit comes under the asymmetrical topologies as the magnitude of dc voltage sources are not equal and are in a particular ratio. This merit of is the fundamental aids in generating a higher number of levels while maintaining same quantity of connected power electronic components. The voltage value of dc voltage source $V_{dc1} = V_{in}$, and for $V_{dc2} = 4V_{in}$.

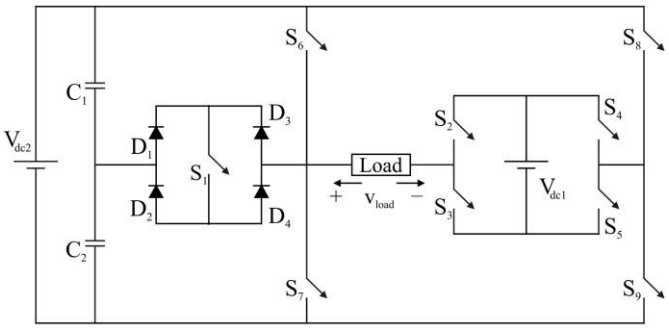

Figure 2. Proposed eleven-level transistor clamped T-Type inverter topology

The switching patterns of this unique topology are shown in Table 1, and it is clear that four devices are required for each level's generation. Traditional eleven-level inverter topologies use 20 switches to create the same output, but this topology only requires nine switches. As a result, switching losses are substantially reduced. It tries to use less power electronic components in this design. The two applied dc voltage sources are connected or disconnected along with capacitor to the load individually or all of them simultaneously. This is done for accomplishing a synthesized voltage waveform across the connected load. In order to achieve it, an appropriate combination of four switches at one time are pushed to the conduction state. This creates several modes for generating a particular voltage level. All the possible modes are shown in Figure 3. Figure 3 (a) and Figure 3 (g) are special modes in which no supply is provided to the load but it can provide

Table 1: Switching table for the Proposed Inverter

Mode	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	v_{load}
1	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	ON	0
2	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF	V_{in}
3	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	$2V_{in}$
4	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	$3V_{in}$
5	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	ON	$4V_{in}$
6	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	ON	$5V_{in}$
7	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	0
8	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	ON	$-(V_{in})$
9	ON	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	$-2(V_{in})$
10	ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	$-3(V_{in})$
11	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	$-4(V_{in})$
12	OFF	ON	OFF	OFF	ON	OFF	ON	ON	OFF	$-5(V_{in})$

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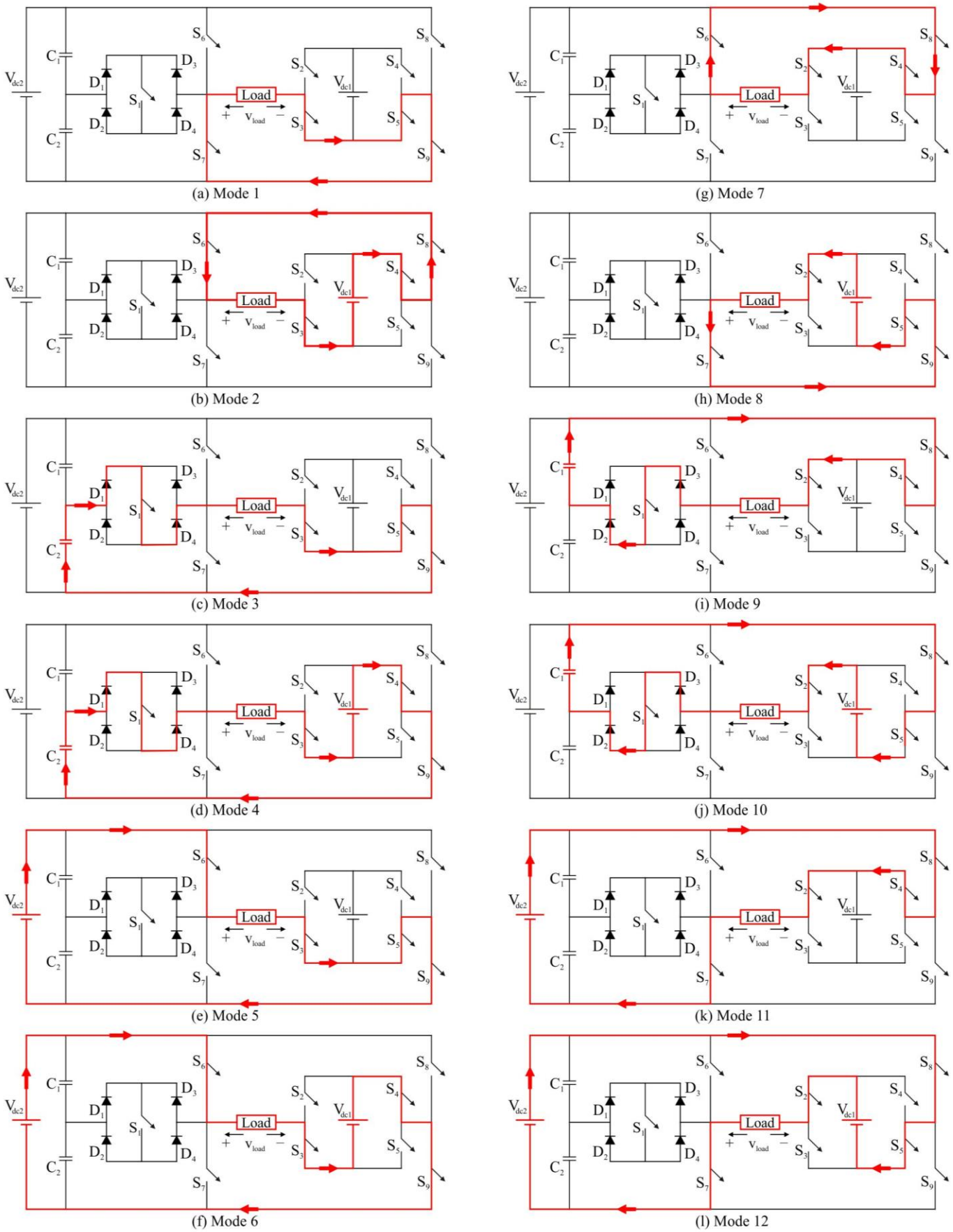

Figure. 3 (a) to (l): Working modes

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freewheeling path for R-L loads. The different equations of this topology are shown in Table 2.

Table 2: Various equations for the proposed topology

Levels	N_L
Total Switches (N_s)	$\left(\frac{9}{10}\right) \times (N_L - 1)$
No of driving circuits	$\left(\frac{9}{10}\right) \times (N_L - 1)$
No of DC Sources	$\left(\frac{1}{5}\right) \times (N_L - 1)$
No of Capacitors	$\left(\frac{1}{5}\right) \times (N_L - 1)$
Total electronics components	$\left(\frac{12}{5}\right) \times (N_L - 1)$

3. MODULATION TECHNIQUE USED

The NLM technique is employed for generating various driving pulses. The sine wave phenomena is at the epicenter of NLM's operation. The NLM approach allows the MLI output to be timed with a sine waveform. This is illustrated in Figure 4.

Each switch's firing angle should be calculated in such a way that when a sine voltage waveform and a multilevel output waveform of equal peak voltage overlap, the sine waveform cuts through the rising edge of the multilevel output at exactly half its amplitude [22]. Figure 4 shows how this works. Because it operates at a low frequency, this approach yields lower switching losses [22]. The following Equations (1) is used to calculate the switching angle.

$$\alpha_i = \sin^{-1}\left(\frac{i-0.5}{n}\right); \text{ for } i = 0, 1, 2, 3, \ldots, n \quad (1)$$

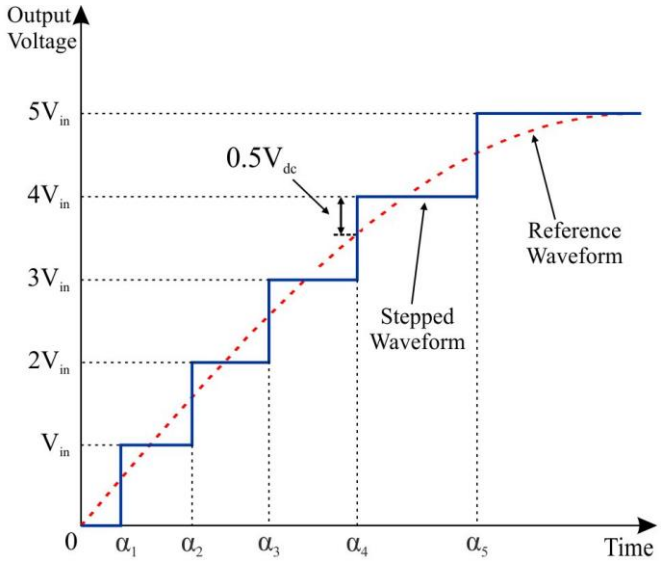

Figure 4. Nearest Level Modulation (NLM) Technique

4. COMPARISON OF PROPOSED WITH CONVENTIONAL AND RECENTLY PROPOSED TOPOLOGIES

Table 3 compares the proposed topology with conventional CHB, NPC, FC's topologies and some recently proposed topologies proposed in [8], [28], [29] and [30] based on the number of switches, the number of DC sources, the number of capacitors required, as well as total number of diodes required. The topology in a prior work [28] has the largest switch count, while the conventional methods require similar count of switches which is less than what is proposed in [28], the topology which is proposed in [29] required less switches than the suggested topology in [28] and the conventional topologies.

Table 3: Comparison of proposed with conventional and recently proposed topologies

Topology	No of Switches	No of Drivers	No of sources	No of capacitors	No of Diodes
CHB-MLI	$2N_L - 2$	$2N_L - 2$	(1/2) (N_L-1)	-	$2N_L - 2$
FC-MLI	2(N_L-1)	2(N_L-1)	(N_L-2)	N_L-1	2(N_L-1)
NPC-MLI	2(N_L-1)	(N_L-1) + 4	(N_L-1)/2	-	(N_L-1) (N_L-2)
[8]	N_L+1	N_L-1	(1/2) (N_L-1)	-	N_L+1
[28]	$2N_L$+4	$2N_L$+4	(N_L-1)/2	-	$2N_L$+4
[29]	N_L+3	N_L+3	(1/2) (N_L-1)	-	N_L+3
[30]	N_L+1	N_L-1	(1/2) (N_L-1)	-	N_L+1
Proposed	(9/10) (N_L-1)	(9/10) (N_L-1)	(1/5) (N_L-1)	(1/5) (N_L-1)	(13/10) (N_L-1)

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The topologies in [8], [30] requires less switches than the topologies just discussed but the proposed topology in this paper has even lower switch count, as shown in Figure 5. The driving circuits requirement also follows a similar trend and it is shown in Figure 6.

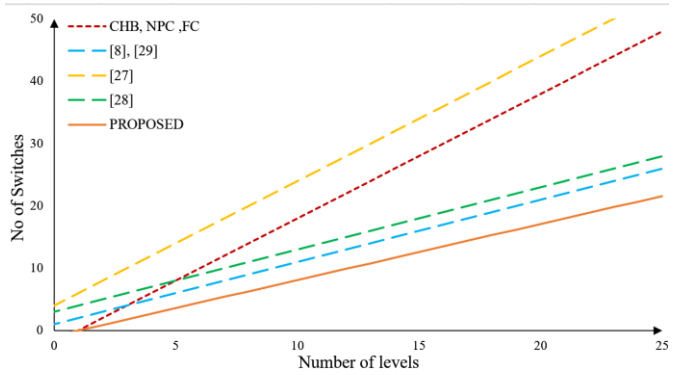

Figure 5. Comparison in terms of number of switches

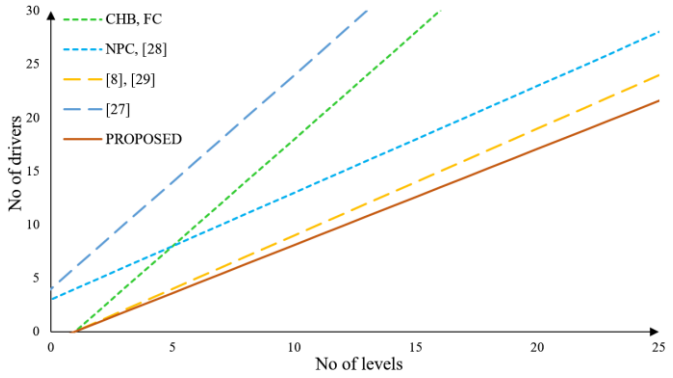

Figure 6. Comparison in terms of number of driving circuits

The usage of DC source requirement for conventional topologies is higher than the recently proposed topologies but in the proposed topology requires even less number of DC sources, it is depicted in Figure 7.

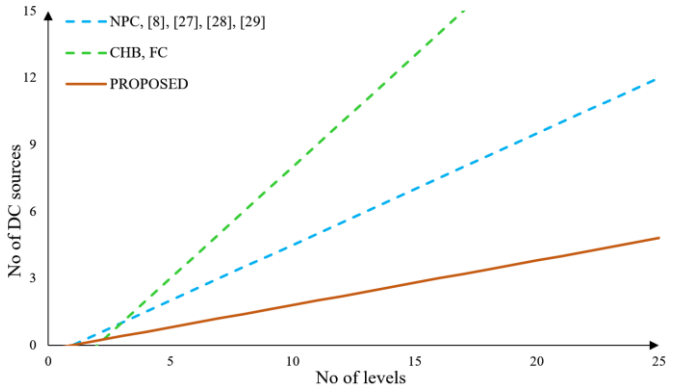

Figure 7. Comparison in terms of number of DC sources

While the traditional eleven-level multilevel inverter uses 20 switches, the proposed structure uses just nine switches to provide the desired output. As a result, decreasing the utilisation of power electronic devices lowers total power dissipation and improves overall system reliability.

5. SIMULATION RESULTS

In order to evaluate the performance of the proposed eleven-level transistor clamped T-type inverter, as depicted in Figure 2, is simulated in MATLAB/Simulink R2021a platform. The MATLAB/Simulink simulation model for this inverter is depicted in Figure 8. IGBT's are used as a switch in the simulation model. NLM technique is employed for the calculation of triggering angles for pushing the IGBTs into the conduction state from the blocking state. The triggering pulses are applied from driver circuit to inverter circuit. The value of used dc voltage sources are V_{dc1}=12V, V_{dc2}=48V which maintains the proportion of magnitudes in 1:4.

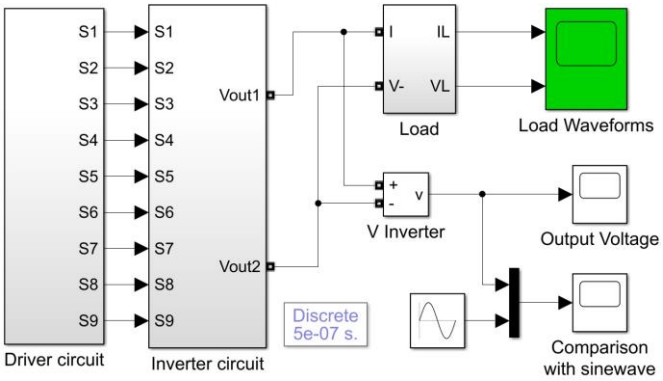

Figure 8. Simulation Model

This model is can generate eleven different voltage levels in step of 12V starting from 0 to a maximum of 60V in positive side and from 0 to -60V in negative side. The load voltage waveform is checked by connecting R-L load with R = 100Ω and L=50mH.

Figure 9 displays output voltage waveform of the simulated model for the proposed eleven-level level inverter

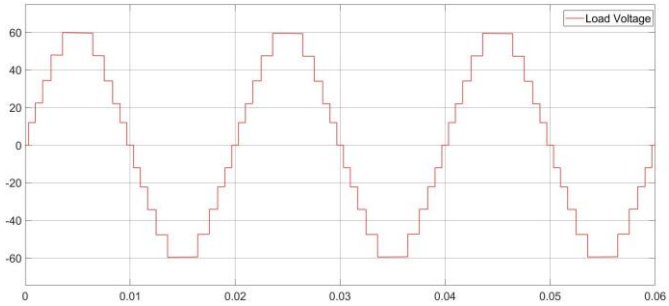

Figure 9. Voltage waveform across load

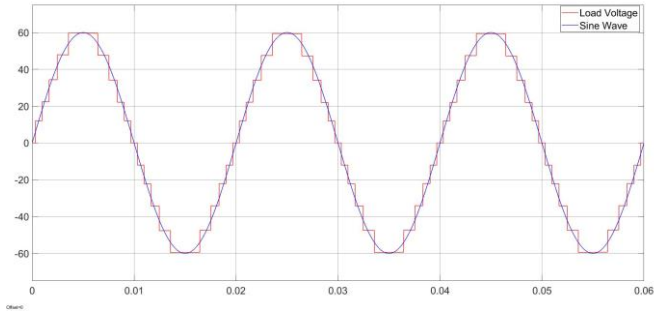

Figure 10. Comparison of load voltage waveform with sine wave

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topology. Figure 10 shows how the load voltage waveform exactly follows the sine wave.

Figure 11 represents harmonic spectrum and magnitudes of distinct harmonic components for output voltage. Based on simulations, the THD of output voltage in this scenario is 4.57%. Figure 12 displays waveform of current flowing through R-L load without output filter.

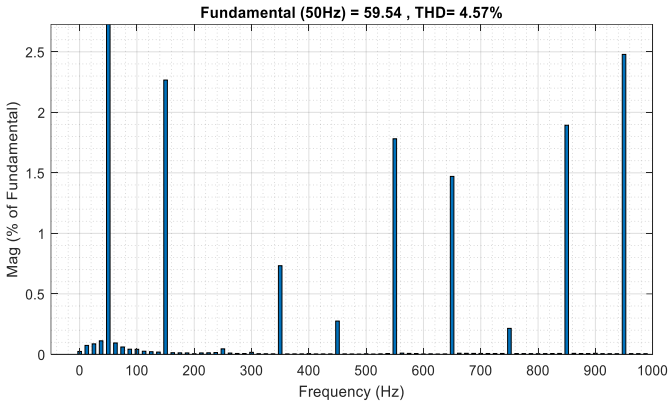

Figure 11. Harmonic spectrum of load voltage

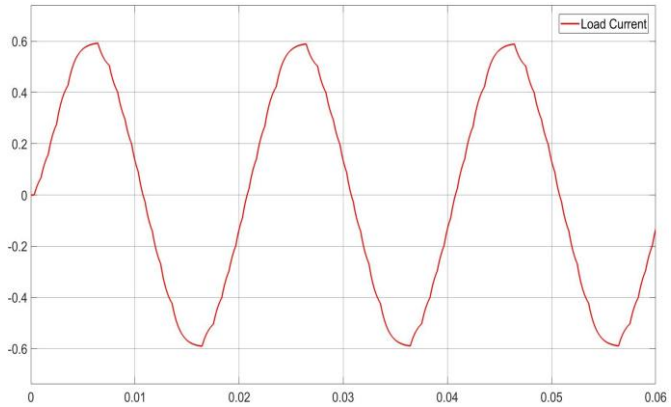

Figure 12. Current flowing through R-L load

Figure 13 depicts related harmonic spectrum for current waveform flowing through the load and as per simulations the value of THD is 2.73% which is very small, hence offers good power quality and it also complies with the IEEE 519 harmonic standard.

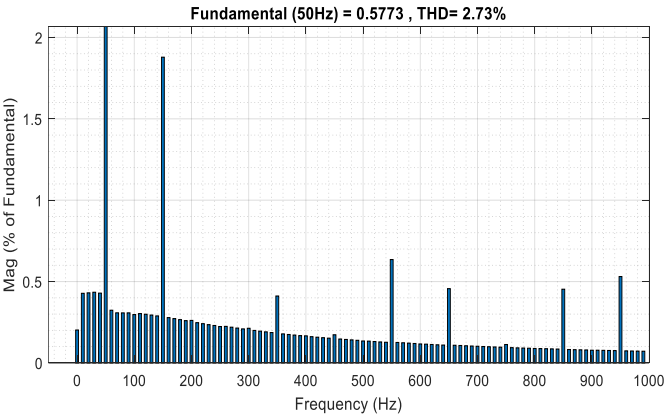

Figure 13. Harmonic spectrum of load current

6. CONCLUSION

In this paper, a new eleven-level transistor clamped T-type multilevel inverter topology is suggested which is asymmetrical in nature. It also has quite superior features over conventional topologies. Some of the features are that requirement of isolated DC voltage sources are reduced in the proposed inverter topology when compared to conventional multilevel inverter topologies along with number of switches and number of driving circuits. These benefits were clearly indicated in the comparison section. NLM modulation schemes is employed for the calculating the switching angles for pushing the switches to conduction state. The simulation of the proposed eleven-level level multilevel inverter topology is simulated in MATLAB/Simulink r2021a with inductive load and its associated results are discussed in this paper. The THD is found out to be in the limits as specified by the standards of IEEE.

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