

Modified Convolution Coding Scheme for Correcting Double Errors

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ABSTRACT

Current communication scenario demands for reliable data transmission at less cost. In recent times, it was found that the application of error correction codes can significantly improve the performance of wireless communication system. Error detection and correction codes play an important role in reliable transmission of data bits over communication channel. There are various error detection and correction codes available. The most commonly used error correction codes are automatic repeat request (ARQ) and Forward error correction (FEC) codes. Many FEC codes have already been designed to improve the performance of communication system. Among all of these, Convolution codes have gained much attention due to its ability of increasing the performance of communication channel. In this paper, we propose a modified convolution encoding scheme in order to improve the double bit error correction capability of the present scheme. Proposed scheme is implemented using MATLAB software. The proposed error correction code capability is investigated considering different modulation scheme namely 16, 32, 64 QAM and 16, 32 PSK. The performance of proposed scheme is compared with that of $\frac{1}{2}$ rate convolution encoded system. It is found that proposed scheme outperforms the $\frac{1}{2}$ rate convolution encoded system with both 16 and 32 QAM modulation. Further, the performance of proposed scheme is studied using 16 and 32 PSK modulation. Moreover, the impact of different constellation number is considered on the performance of proposed scheme encoded system.

Keywords: EDAC, Convolution codes, Forward Error Correction codes, QAM, PSK

1. INTRODUCTION

Today's world demands for reliable data transmission techniques that are suitable for wireless communication. There is an increasing need to transmit data reliably and quickly. Due to ever growing demand of reliable data transmission researchers are continuously working to find new techniques that can send information correctly and quickly. For transmission of data, a channel or transmission medium is necessary. But while transmission of data signals through transmission channel information get distorted due to various channel impairments. Especially in wireless communication system, the main problem of concern is multipath fading which leads to degradation of the signal in the terms of bit error rates. Multipath fading greatly reduces the efficiency of wireless communication system. It is necessary to allow these systems to achieve their utmost performance by developing new techniques. Error detection and correction codes [1,2] lead to much improvement in the performance of wireless communication system. This is the reason these error detection and correction codes has gain much popularity in the field of wireless communication scenario. Error detection and correction codes[3,4] works on the principle of sending the data in the form of coded sequence and then retrieving the original data from the received data bits. These error control codes play an important role in wireless communication systems. First error detection and correction code is developed by American mathematician Richard Hamming named Hamming code [5]. There are many error-correcting codes such as Convolutional codes [6], Golay codes [7,8], Low-

density parity-check codes[9,10] etc. The literature of EDAC schemes is vast but on the broad level, EDAC schemes can be classified into two types –automatic repeat request (ARQ) and forward error correction (FEC). In ARQ [11] data is retransmitted again and again until sender receive positive acknowledgement from the receiver. Hence ARQ is not suitable choice when signal is to be transmitted through noisy channel. In such cases, FEC[12,13] is a more suitable method for EDAC in communication. The mostly implemented error correction code is forward error correction code. FEC leads to increase in number of transmitted bits by a factor of code rate. These extra inserted bits provide more robustness against the errors occurring in transmission channel. The key, then, is to find a way to make best use of these extra bits. These redundant bits are systematically generated from information data. Input data bits are sent to the encoder and encoder codes the input data according to error control code used. The output of the encoder is a code word for the input data. The length of the code word is greater than original data [14]. After this, code-word is sent through the communication channel. During transmission of the coded data through communication channel, data may get distorted. At the receiver side, distorted data is sent to the decoder which decodes the received data and produces the original input data. The capability of the error control code depends upon its ability to detect and correct the error introduced in the transmitting information through communication channel[15].

The most widely used forward error correction scheme is convolution encoding [16-17]. The convolution encoding scheme provide a large improvement in the performance of wireless communication system as compare to uncoded

system. Convolution encoder consists of shift registers and modulo2 adder. Initially the encoder is in 00 state. When input bits are sent then modulo 2 adder performs its function and output bits are generated [18]. After this bits are shifted sequentially to obtain output bits or code word for the input bits. Convolution encoder can be represented by state diagram, tree diagram or trellis diagram. Trellis diagram is generally preferred over both tree and state diagrams because they represent the sequence of occurring of events. Along x-axis time of occurrence of a bit is plotted and all possible states of the encoder are marked on the y-axis. Number of possible states is 2^L , where L is number of memory registers used for encoding. Diagram of $\frac{1}{2}$ code rate convolution encoder with two memory registers (Constraint length = 2) is given below:

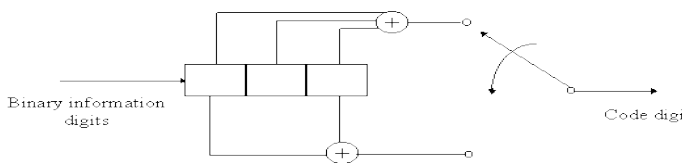


Fig. 1A $\frac{1}{2}$ code rate convolution encoder

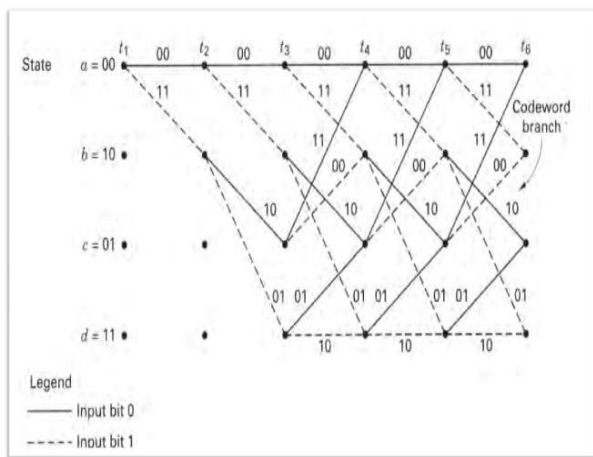


Fig. 1B: Trellis Diagram of convolution encoder

The advantage of FEC codes is that they do not require re-transmission of original data. Hence, reverse channel is not required [19]. It must be mentioned here that FEC code improve the performance of communication system at the cost of increased band width. Further, FEC codes add to the complexities of the hardware used in the communication system. Rest of the paper is organized as: Section 2 introduces proposed error detection and correction scheme that leads to decrease in BER during transmission. Section 3 explains the advantages of proposed scheme over the convolution encoder scheme. The implementation of proposed scheme using MATLAB software and results are presented in section 4. Finally, section 5 concludes the paper.

2 MODIFIED CONVOLUTION CODES FOR DOUBLE ERROR CORRECTION

Convolution codes are most widely implemented error correction codes. From, the trellis diagram of convolution codes, it is clear that two possible outputs at each node are either 00,11 or 01,10. Hence, when two bit errors are

introduced by the transmission channel, the error correction capability of convolution code falls down. Another drawback of the convolution codes is that the performance of the convolution codes decreases with the decreasing constraint length. Hence, to achieve better performance, codes with large constraint length must be implemented. But increasing constraint length leads to increase in the decoding complexity as well as increase in the decoding time. This paper is an attempt to combat these drawbacks of the convolution codes and to make them more robust against double consecutive errors with less constraint length.

2.1 Proposed encoder is a $\frac{1}{2}$ rate encoder which consists of 2 registers and 1 modulo2 adder. The idea is to send the modulo2 adder of two bits at the place in between them i.e. codeword consists of original data bits at odd places and modulo 2 adder of input bits at even places. For example, modulo2 adder of 1st and 2nd input bit is placed at 2nd position of code word and so on. This can be explained as follows: -

Encoder consists of two registers. First register represents the state of the encoder and second register consists of incoming bit. Both register are connected with modulo2 adder. Initially the encoder is in state 0. At $t=0$, incoming bit enter in the 2nd register and modulo2 adder performs its function. After the modulo2 addition, bit is shifted to left so that output consists of output bit from shift register followed by the result of modulo2 adder. Hence, for one bit input output consists of 2 bit. For example, if input bits are 1010, then output of the encoder will be 01 11 01 11 00.

It must be mentioned here that the modified convolution encoder is of constraint length 1. Hence, consist of two memory states 0 and 1. Also, the generator polynomial of the modified scheme is [0 1] and [1 1] instead of standard generator polynomials of convolution codes [1 0], [1 1]. In Section 2.1b it is shown that this modification leads to much change in the trellis diagram of the encoder.

2.1.a Impulse response: Codeword for input bit can be obtained from the inner product of incoming bit with the impulse response of the encoder for that bit. Suppose the bit 1 is to be encoded by proposed encoder.

At $t=0$, state of the encoder is 0 and input bit is 1. Modulo2 adder would be 1. Hence the output bits will be 01. And input bit 1 shifted to left.

At $t=1$, state of the encoder will be 1 and input bit is 0. Modulo2 adder will results into 1. Hence, the output bits will be 11 and state of encoder makes transition to state 0.

At $t=2$, state of the encoder is 0 and 0 bit is sent to the encoder. After modulo2 addition the output bits will be 00. Hence, impulse response of the encoder for bit 1 is 01 11 00.

Impulse response of the encoder for bit 0 will be 00 00 00. With the help of this impulse response, codeword of any input bits can be found. For example, the codeword of 1010 can be found as follows. Write the impulse response of each incoming bit shifting to left each time. And then, perform modulo2 addition. Result will be the corresponding code word.

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Incoming bit	Impulse response					
1	01	11	00			
0		00	00	00		
1			01	11	00	
0				00	00	00
Code word	01	11	01	11	00	00

Table 1: Coding the input data using impulse response of 0 and 1 bit.

Hence, the code word for the input bits 1010 is 01 11 01 11 00 00. It is observe that state of encoder makes a transition from state 0 to 1 or from 1 to 0 at the arrival of incoming bit. Incoming bit decides the state in which the encoder will reside after that bit. Table given below represents how the encoder will makes transitions from one state to another.

Initial state	Incoming bit	Output bits	Final state
0	0	00	0
0	1	01	1
1	0	11	0
1	1	10	1

Table 2: Transitions of the encoder from one state to other on arrival of input bit

2.1.b Description of the proposed encoder

- i) State diagram
- ii) Trellis diagram

i) State diagram: - At any time, encoder can exist either in state 0 or state 1. At each state only two events can occurs either the arrival of '0' bit or '1' bit. For example, if encoder is in state 0 and incoming bit is 1 then encoder will make a transition to state 1 and output will be 01. In the diagram, solid line represents the event of incoming bit to be 1 and dashed line represents the transition of state when incoming bit is 0. The bits written above the line represents the output bits when corresponding transition occur.

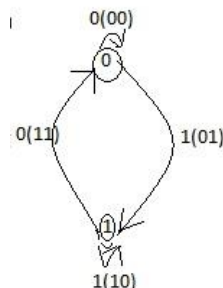


Fig2: State diagram of the Proposed Encoder

ii) Trellis diagram: - Trellis diagram is another way to represents the encoder. Two possible states of the encoder are written along vertical axis. At the arrival

of each bit, we move horizontally. Each transition can occur either by the arrival of '0' bit or '1' bit.

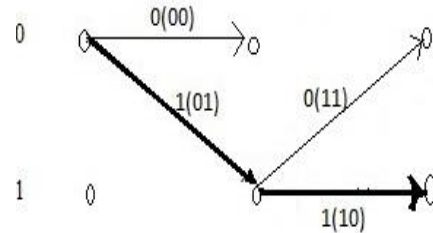


Fig3: Trellis diagram of the Proposed Encoder

The bits outside the parenthesis represents incoming bit and inside the parenthesis represents output bits. This is worth noting that the possible output bits at the each node of the modified encoder are 00,01 or 11,10. Hence, when two bit error occurs in the received bits, possible bits do not change into one another and can be detected. While for the conventional convolution codes the possible bits at each node are 00,11 or 01,10. That can not be detected in case of two bit errors.

2.2 ENCODING OF INPUT BITS USING PROPOSED ENCODER

By using the proposed encoding scheme for encoding of input data bits, the number of transmitted data bits gets doubled as compare to that of input bits (ignoring the flush bits). Let the input data bits be a row vector of dimensions $1 \times N$, N is number of input data bits to be sent. After encoding, the encoded bit stream becomes a row vector of dimensions $1 \times 2N$. To encode the data bits with the proposed encoder, the following algorithm should be followed:

- i) Consider data bits in the form of a row vector of length N where N is number of data bits to be sent through the communication channel.
- ii) Set the initial state of the encoder to be 0. Insert the input bit into the 2nd register. Compute the modulo2 adder of two bits using the following table

Bit 1	Bit 2	Output
1	1	0
1	0	1
0	1	1
0	0	0

Table 3: Truth table of modulo 2 adder

iii) Output bit stream consists of input bits and modulo2 adder of the bits such that n^{th} input bit placed at $(2n+1)^{\text{th}}$ position in output bit stream and modulo2 adder of n^{th} and $(n+1)^{\text{th}}$ input bit at $(2n+2)^{\text{th}}$ position of output bit stream, where n varies from 1 to length of input bit stream. First two bits of output bit stream consist of initial state of the encoder i.e. 0 bit followed by modulo2 adder of 0 bit and first input bit. This result in output stream of length $2N$ (ignoring flush

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bits). An example for encoding input bit stream of length 4 using proposed encoding scheme is explained as follows:

- i) Consider an input bit of length 4 be $X = [1\ 0\ 1\ 0]$.
- ii) Set the initial state of encoder be 0. Input bit 1 is inserted in the 2nd shift register. Then, modulo2 adder performs its function and computes the result to be 1.
- iii) The output consists of bit from the state register followed by modulo2 adder. So, the output bits will be 01. The process is repeated up to the length of input bits. The output become 01 11 01 11 00 00. Here, last 4 bits 00 00 are flush bits.

2.3 DECODING OF RECEIVED DATA BITS

Reconstruction of original data bits from received data bits can be done with the help of the following decoder. Viterbi decoding can be used for decoding the received data bits. To retrieve the original data bits using Viterbi decoder scheme, the following algorithm should be used:

- i) Construct a null distance matrix of dimensions $2 \times N + 1$ and a null metric matrix of dimensions $4 \times N$. Here, N is number of input bits that are sent together in the form of a block.
- ii) Compute elements of metric matrix which is the norm of (0, 0), (0, 1), (1, 0) and (1, 1) from the simultaneous elements of row vectors y_0 and y_1 . Here, y_0 is the stream of odd placed and y_1 of even placed bits of received data.
- iii) Computation of distance matrix: compare the metrics of all the paths that converges to a node in the trellis diagram of proposed encoder. Then, the elements of distance matrix is the distance of the path for which metric is minimum.
- iv) The elements of $N + 1$ th column of distance matrix are compared and the path of minimum distance is kept. Decoded bits are computed according to trellis diagram.

3 MERITS OF PROPOSED MODIFIED CONVOLUTION ENCODER OVER CONVOLUTION ENCODER

Proposed scheme has several advantages over the conventional convolution scheme. These are mentioned below.

- i) It must be noted from the trellis diagram of modified convolution encoder, at each node one of the two pairs of output is possible either 00,01 or 10,11. All the four outputs are not possible at any node. It must be mentioned that in case of convolution encoder pairs that are possible at each node are 00, 11 and 01, 10. If 2 bit error occur during transmission of data through transmission channel then two possible outputs at each node of convolution encoder changes into one another. Hence, the two bit error will not be detected by the convolution encoder. But in our modified convolution encoder if 2 bit error occurs during transmission then two possible outputs at each node will not changes

into one another. Hence, error will be detected and corrected by the decoder.

- ii) Since the constraint length of the modified convolution encoder is only 1. So, the decoding complexity is very less.
- iii) The simulation time for the proposed scheme coded system is less than the convolution scheme.

4 RESULTS AND DISCUSSION

The simulation of proposed scheme is done using MATLAB software. Information data is encoded using proposed encoder. Then modulation of encoded data is done. QAM and PSK modulations have been used for simulating the proposed model. Modulation converts the encoded data into complex form. In this paper, two types of modulations are used for modulating the encoded data. QAM and PSK (and their higher orders) modulation is used in this paper. Modulated data is send over AWGN channel. Channel introduces error to the encoded data and encoded data gets distorted. At the receiver side, first demodulation of received data is done. After demodulation, proposed decoder is used for decoding. Performance of proposed scheme is studied in terms of Bit Error rate (BER) as the function of SNR (E_b/N_0 in dB) over AWGN channel. BER performance of proposed scheme is compared with that of $\frac{1}{2}$ rate convolution encoded system with constraint length of 2. The generator polynomials for the conventional scheme is [1 1 1], [1 0 1].

Parameters used for simulation are

Parameter	Convolution encoder	Proposed encoder
Number of input bits	100000	100000
Number of bits per block	1000	1000
N sampling	1	1
Code rate	$\frac{1}{2}$	$\frac{1}{2}$
E_b/N_0 in dB	0 to 15	0 to 15
Type of modulation	16-QAM, 32-QAM, 16-PSK, 32-PSK	16-QAM, 32-QAM, 16-PSK, 32-PSK

Table 4: Simulation Parameters used

Fig 4 represents the performance of Convolutional encoded and proposed scheme encoded systems using 16-QAM modulation over AWGN channel. It is clear from the graph that proposed scheme performs better than $\frac{1}{2}$ rate convolution encoder especially in low E_b/N_0 range. Fig 5 shows the BER performance of proposed scheme encoded and convolution encoded systems using 32-QAM modulation.

AWGN channel is used as transmitting medium. This is clear from the results that proposed scheme outperforms than convolution encoder.

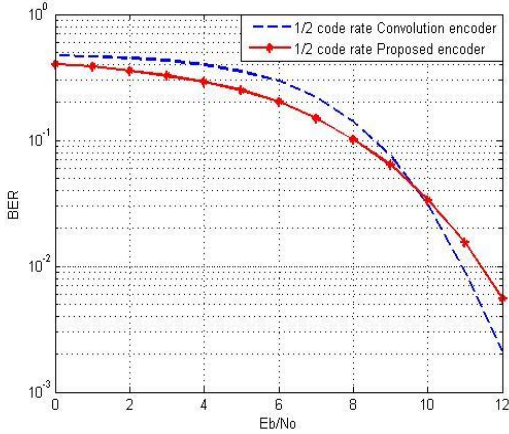


Fig 4: Performance of Proposed scheme encoded and convolution encoded system using 16-QAM modulation

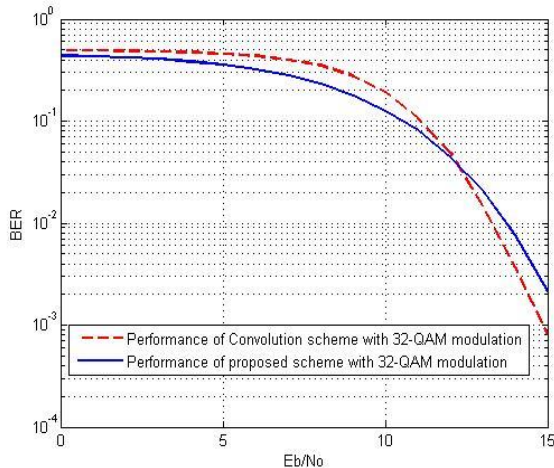


Fig 5: Performance of Proposed scheme encoded and convolution encoded system using 32-QAM modulation

Fig 6 depicts the performance of proposed scheme using 16-QAM, 32-QAM and 64-QAM modulations over AWGN channel. It is clear from the graph that with the increase in order of modulation, performance of proposed scheme decreases. In other words, proposed scheme performs better with lower order of modulation. For example, to achieve BER of 10^{-1} , 16-QAM modulated system require 8 dB of E_b/N_0 while 32 and 64-QAM modulated systems require 10 and 14 dB of E_b/N_0 value. This is clear from this observation that performance of proposed scheme is better with 16-QAM modulation.

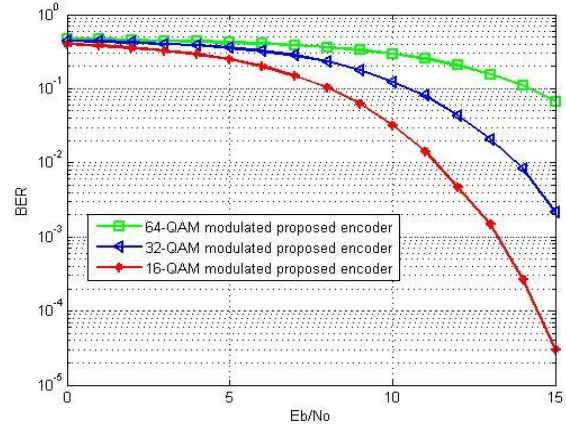


Fig 6: Performance of proposed scheme encoded system using 16, 32 and 64 QAM modulation

Fig 7 represents the performance of proposed scheme and convolution encoder using 16-QAM and 16-PSK modulation over AWGN channel. It is clear that proposed scheme performs better with QAM modulation. The E_b/N_0 value require for achieving a particular BER is less with QAM modulation than that require with PSK modulation. For example, to achieve BER of 10^{-1} , proposed scheme with 16-QAM modulation require 8 dB while with 16-PSK modulation proposed scheme require 11 E_b/N_0 value. Hence it is clear that performance of proposed encoder is better with 16-QAM modulation than that with 16-PSK modulation.

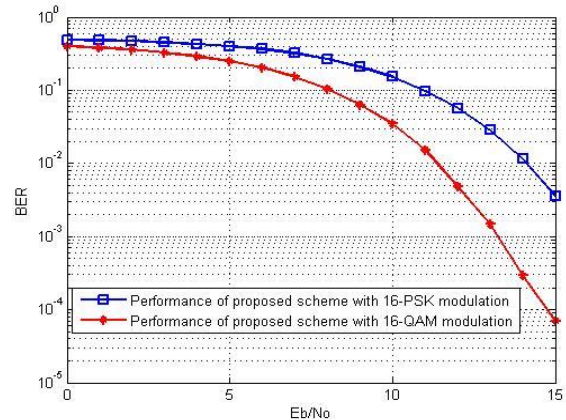


Fig 7: Performance of proposed scheme encoded system using 16 QAM and 16- PSK modulation

Fig 8 depicts the impact of different orders of PSK modulation on the performance of proposed scheme. Studies show that performance of proposed scheme is better with 16-PSK modulation than with 32-PSK modulation. Proposed scheme performs better with lower order of modulation scheme.

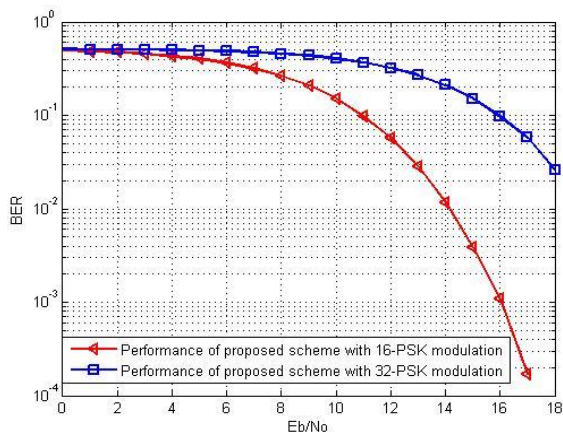


Fig 8: Performance of proposed scheme encoded system using 16 and 32 PSK modulation

5 CONCLUSIONS

In this paper, we have proposed a modified convolution codes that are particularly suitable for two bit error corrections with one memory register. Various ways of representing the proposed encoder has been presented. Proposed scheme is simulated using MATLAB software and results are shown in the paper. Performance of proposed scheme is represented in terms of BER v/s Eb/No. Performance of proposed scheme is compared with that of convolution encoded system with two memory registers. It is shown that proposed scheme with one memory register performs even better than convolution encoded scheme with two memory registers particularly in low Eb/No range. It is also shown that proposed scheme performs better with lower order of modulation. The performance of proposed scheme is studied using 16-QAM, 32-QAM and 64-QAM modulations. Results shows that proposed scheme performs better with 16-QAM modulation over AWGN channel. Performance of proposed scheme using 16-QAM and 16-PSK modulation has been compared. It is found that proposed scheme perform better with 16-QAM modulation. Different order of PSK modulation has been used to modulate the proposed scheme encoded data bits. Here, it is found that performance of system increases with decrease in order of modulation.

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