Volume 8, Issue 5
October 2019

ITEE Journal
Information Technology & Electrical Engineering

ISSN: - 2306-708X



# A Wide Tuning Range Self-Switched Biasing VCO in 0.18µm CMOS Technology

**[1]R. C. Gurjar and [2]D. K. Mishra**

[1]Department of Electronics & Instrumentation Engineering, SGSITS, Indore

[2]Department of Electronics & Instrumentation Engineering, SGSITS, Indore

E-mail: [1]rcgurjar94@gmail.com, [2]dmishra@sgsits.ac.in

## ABSTRACT

A novel self-biased LC Voltage Controlled Oscillator is presented in this paper. Proposed self-biasing provides improvement in phase noise. An IMOS varactor for tuning the operational frequency is employed in the proposed design. The simulation result shows that proposed VCO achieves a frequency turning range (FTR) of 25% and a phase noise of -120 dBc/Hz at 1 MHz offset frequency from carrier. The VCO consumes 3.118 mA from 1.8 supply voltage.

**Keywords:** CMOS, IMOS, LC Voltage Controlled Oscillator, Low Phase Noise, Tuning Range

## 1. INTRODUCTION

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With the explosive growth in today's comm system, a demand for high performance VCO (Voltage Controlled Oscillator) is desirable for radio-frequency integrated circuit (RFIC). The VCO which is used for the down-conversion and up-conversion of RF signals is an important block of transceiver. Due to poor phase noise performance, ring oscillator are rarely used in RF systems. So LC-VCOs are preferred than ring oscillators. A VCO is an oscillator whose oscillation or working

frequency (shown in figure 1) can be modified using an external control voltage. It is important the way the frequency of the VCO varies when control voltage changes. A voltage controlled oscillator is a circuit whose output frequency is a liner function of its tuning.

$$\omega_{out} = \omega_o + K_{VCO}V_{cont} \quad (1)$$

Where $K_{VCO}$ is VCO gain, $V_{cont}$ is control voltage, $\omega_{out}$ is the output frequency, $\omega_0$ is the frequency of the output signal when $V_{cont}$ is zero and $\omega_1$, $\omega_2$ shown in figure 1 are the frequencies between which tuning can be achieved. However practically the tuning characteristics of the VCO are nonlinear and hence the VCO gain is not constant. The performance evaluation of the VCO may differ based on applications and the mode of operation. Tuning range decides the output frequencies which can be generated linearly. Output spectrum is very important and must be noiseless. As the output signal purity is the main concern of the designer, the amplitude and noise contained in the output are the major parameters which decide its quality. Phase noise prediction and low noise design is the most important part of the VCO design. Like in any other design, power consumption is a very important concern of VCO. Implementation of VCO in different technologies and topologies for different applications continue to challenge designers. VCO may be realized with many configurations according to the applications and performance requirements. Ring Oscillator, LC oscillator, Relaxation Oscillators are the available fundamental topologies. This paper is organized as

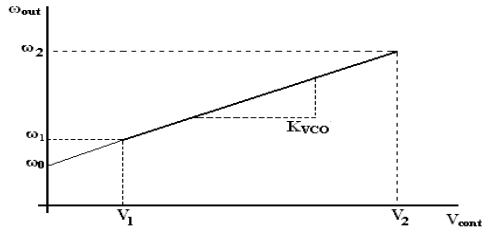


Figure 1: Ideal VCO Characteristics

follows: first we present the circuit design consideration used to minimize the phase noise and widen the tuning range, then we show the realization of MOS varactor followed by the simulation results. Finally we conclude the paper with a performance summary and comparison with start of art designs.

## 2. VCO DESIGN AND IMPLEMENTATION

In Several different cross-coupled LC VCO topologies have been proposed. Complementary cross coupled topology shown in fig.2 (a) is popular due to its ability to reduce flicker noise [1]. Negative resistance is required to cancel out the parasitic resistance of LC tank.

$$R_{neg} = \frac{-2}{g_{mn}+g_{mp}} \leq R_{eq} \quad (2)$$

Double cross coupled differential provides sufficient negative resistance to cancel out losses in the LC resonator. The LC VCO proposed (shown in fig. 2.b) in this paper is a type of cross –coupled which consists of PMOS and NMOS transistors. For a symmetrical VCO W/L ratio of PMOS transistor is chosen 2.5 times that of NMOS. Channel lengths of transistors are chosen minimum to lower parasitic capacitance and achieve the maximum transconductance.

The inductor of value 5nH in proposed design is taken from the 0.18um design kit. By varying the number of turns and diameter of metal structure, inductor value can be changed.

Volume 8, Issue 5
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ITEE Journal
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Selecting the inductor from design kit provides an excellent model because it has been tested and developed by the vendor.

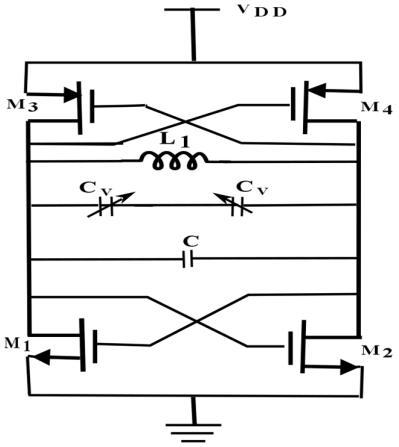


Figure 2(a): Conventional LC VCO

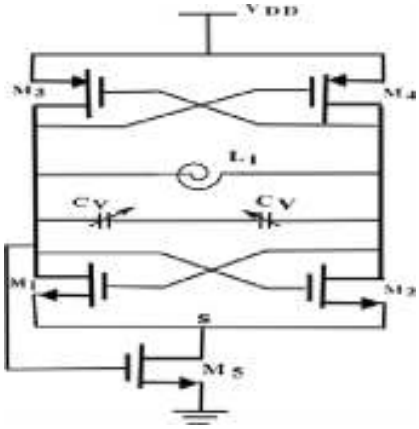


Figure 2(b): Proposed Self Switched Biased VCO

The next important parameter in designing VCO is its phase noise. Phase noise can be reduced in several ways [1]-[2]. Phase noise generation mechanism for VCOs has been thoroughly analyzed in [13, 15] To model the phase noise, Lesson's (3) is used.

$$L(\Delta\omega) = 10log\left[\frac{2FKT}{P_{sig}}\left\{1+\left(\frac{\omega_o}{2\Delta\omega Q}\right)^2\right\}\left(1+\frac{\Delta\omega_{1/f3}}{|\Delta\omega|}\right)\right] \qquad (3)$$

Where $\Delta\omega$ is frequency offset from output frequency in Hz, $L(\Delta\omega)$ = Phase Noise in dBc/Hz, $\omega_o$ is output frequency in Hz, $\Delta\omega_{1/f3}$ is the flicker noise corner frequency in Hz, Q is loaded quality factor of LC resonator, K is Boltzmann's constant , F is noise factor, T is temperature in Kelvin, $P_{sig}$ is the oscillator output power. One way to reduce the phase noise involves remove the bias circuitry completely from the VCO circuit [8]. By removing the tail current generator, now $1/f^3$ noise of the oscillator can originate from the flicker noise of the MOS Transistor Switches. To reduce the flicker (1/f) noise contributed by MOS switches, device area can be increased as (4) shows

$$\overline{i_{n,1/f}^2} \propto \frac{K}{WL} \qquad (4)$$

The value of K for PMOS is 50 times lower then NMOS, so for designing the varactor in the proposed VCO, PMOS transistors have been used.

The Close-in phase noise of VCO is mainly determined by the flicker noise of the tail transistor. As the size of transistor in newer CMOS process tend to have lower value, so flicker noise will increase. In this paper, self-switched biasing technology is used to reduce the flicker noise from tail biased transistors. Switching of a tail transistor from inversion to accumulation by applying a sine waveform will help in lowering the flicker noise [11]. The switched biased technique has been confirmed by many published papers [8]-[13]. VCOs can use their own oscillation waveform for the switching of the tail transistor [10]. In the proposed design, it is difficult to cycle the tail transistor $M_5$ from strong inversion to accumulation. So it is cycled from strong inversion to weak inversion.

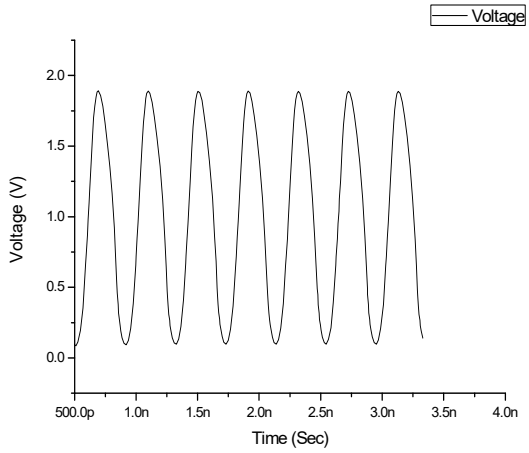


Figure 3(a): Transient Gate-Source Voltage (Vgs) across $M_5$

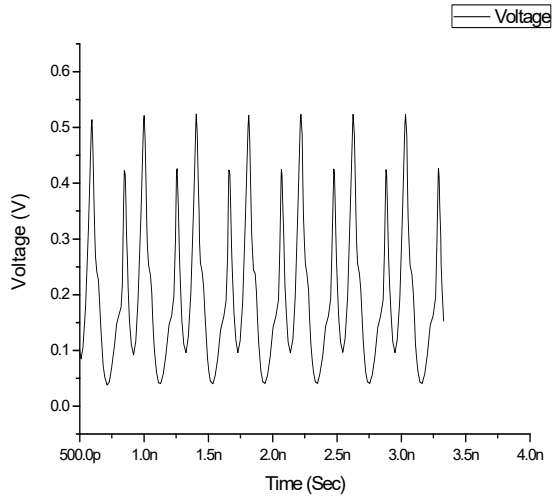


Figure 3(b) Transient Drain-Source Voltage (Vds) across $M_5$

As shown the simulated waveform in fig. 3, the high level of $V_{gs}$ (Shown in fig.3.a) is larger than the threshold voltage ($V_{tno}$ = 0.307) of $M_5$, it will work in strong inversion. When low level of $V_{gs}$ is lesser than the threshold voltage of

Volume 8, Issue 5
October 2019

ITEE Journal
Information Technology & Electrical Engineering

ISSN: - 2306-708X



$M_5$, it will work in weak inversion. So cycling of $M_5$ between the strong inversion to weak inversion gives the improvement.

## 3. MOS VARACTOR

MOS varactors are variable capacitors established by the MOS structures. The inductor L and varactor C along with parasitic capacitance generates an approximate oscillation frequency (f)

$$f = \frac{1}{2\pi\sqrt{L_{tank}\ (C_V + C_P)}} \quad (5)$$

Where $C_V$ is the varactor capacitance and $C_P$ is the equivalent parasitic capacitance associated with the input/output buffer, interconnect wires and device capacitance.

The tuning range depends on the ratio of Maximum capacitance ($C_{max}$) and minimum capacitance ($C_{min}$) of the Varactor. For varactor based oscillator Cmax/Cmin becomes small because of the parasitic capacitance which is having a fixed value. So in the proposed topology, additional fixed capacitor is not used. Design of varactor and simulated capacitance-tuning voltage characteristics of a single MOS transistor are shown in fig.4 (a&b).

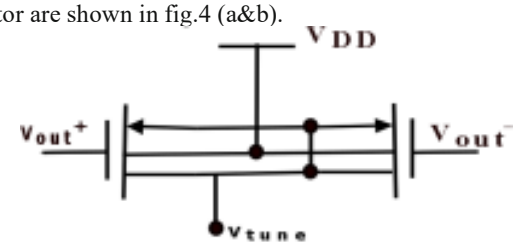


Figure 4(a): Proposed Varactor

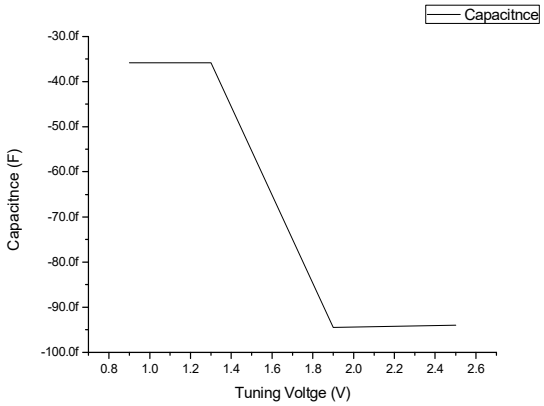


Figure 4(b): Simulated Varactor Capacitance Vs Tuning Voltage

The source and drain are connected as one terminal of the varactor and gate as other. Body terminal of MOS is connected to supply voltage. Because the bulk is connected higher or equal potential with that of gate, this structure works only in inversion mode and referred as IMOS varactor. In the proposed varactor , two MOS varactor in series is parallel to other two varactor which are in series connection. This varactor in parallel with inductor constitute the tank circuits. As the gate node of varactor is having a signal swing, the instantaneous value of capacitance changes throughout the signal period. Large signal analysis of MOS varactor is reported in [3], [14]. If the output oscillator output voltage is sinusoidal at resonant frequency $f_0$, then the average capacitance can be expressed as [14]

$$C_{AVG} = \frac{(rms(i))_{f_0}}{rms\left(\frac{dv(t)}{dt}\right)_{f0}} \quad (6)$$

Where rms(i) is the root mean square value of current of period signal of oscillator and v(t) is the time varying voltage of the oscillator.

## 4. SIMULATOIN RESULTS

We have designed the proposed VCO in UMC 0.18µ CMOS technology and used cadence spectre simulator. The circuit generates the stable periodic output as plotted in fig. 5. IMOS varactor has been designed and Capacitance – Tuning Voltage characteristics of a single MOS is shown in fig. 4(b). To see the actual impact of the MOS- varactors on the output frequency, the 4 IMOS varactors from fig. 4(a) were connected parallel and implemented in the LC-tank VCO. Frequency tuning curve of the LC-VCO with an inversion-mode varactor is shown in fig.6. The oscillation frequency ranges over 2.0- 2.5 GHz as the tuning voltage of the varactor is changed from 0.5 to 2.5V. A Comparison between this work and state of the art oscillators is shown in Table II.

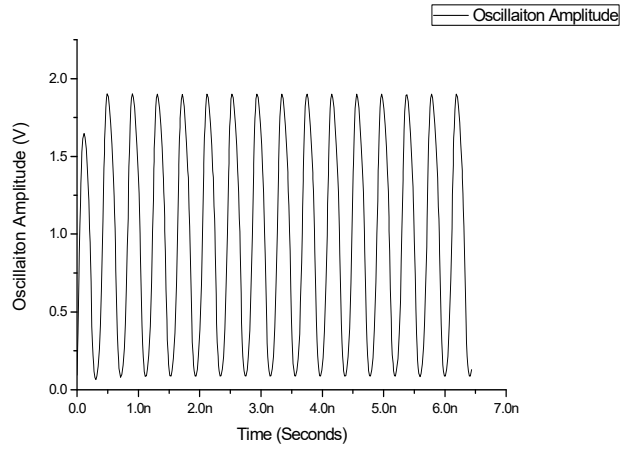


Figure 5: Simulated time domain Output waveform

As shown in fig. 7, the phase noise at 1MHz is less than -120 dBc/Hz. Fig. 8 shows the output power of 12.4 dBm at 2.8 GHz. To evaluate the performance of the proposed VCO, The figure of merit (FOM) defined in eq. (7) is widely used.

$$FOM = L(f_{off}) - 20\log\left(\frac{f_o}{f_{offset}}\right) + 10\log\left(\frac{P_{DC}}{1mw}\right) \quad (7)$$

Where $L(f_{off})$ represents the phase noise at the offset frequency from the carrier frequency $f_o$ and $P_{DC}$ is the dc power dissipation in mW.

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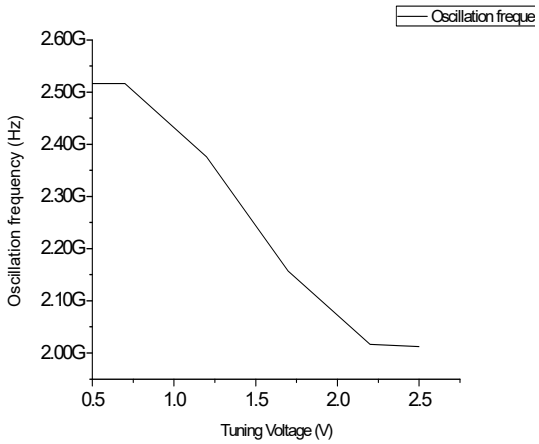


Figure 6: frequency vs. tuning voltage curve

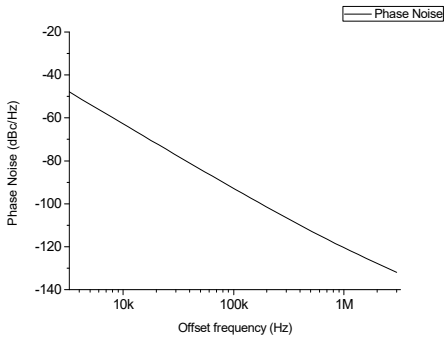


Figure 7: Simulated Phase Noise

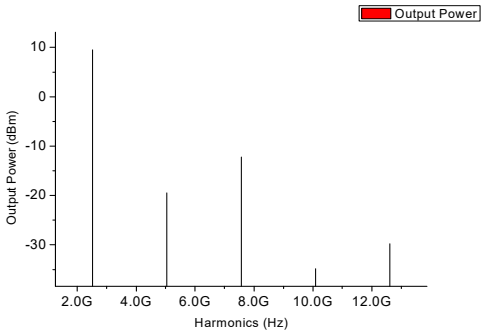


Figure 8: Output Power Spectrum

TABLE I: SUMMERY OF SIMULATION RESULSTS FOR THE PROPOSED VCO

| | |
|---|---|
| Technology | 0.18 μm UMC |
| Supply Voltage | 1.8 V |
| Tuning Range | 2.00 to 2.5 GHz |
| Phase Noise | -120 dBc/Hz @ 1MHz,<br>-130 dBc/Hz @ 3MHz |
| Power Dissipation | 5.61 mW |
| Output Power (dBm) | 12.4 |

TABLE II: COMPARISION OF VCO PERFORMANCE

| References | This Work | [7] | [6] | [5] | [4] |
|---|---|---|---|---|---|
| Process Technology (μm) | 0.18 | 0.18 | 0.13 | 0.09 | 0.18 |
| Supply Voltage (V) | 1.8 | 3.3 | 2.30 | 0.75 | 1.2 |
| Output Freq (GHz) Tuning Range (%) | 2.0 - 2.5 (25) | 4.64 - 5.3 (12) | 5.79 - 6.72 (14) | 37.5-41.0 (8.9) | 2.28-2..59 (12.2) |
| Phase Noise (dBc/Hz @ 1MHz) | -120 | -118 | -124 | -96.7 | -125 |
| Power Dissipation (mW) | 5.61 | 1.44 | 2.25 | 1.65 | 1.9 |
| FOM (dBc/Hz) | -180 | 190.4 | -193 | -186.3 | -190 |

## 5. CONCLUSION

VCO is most important building block of RF transceivers since there performance affects the overall transceiver performance. Varactors are the tuning component of the LC VCOs and play an important in deciding the tuning range of VCO.A wide tuning range LC VCO with self-switched biasing is reported. The VCO operates from 2.0 to 2.5 GHz with 25% tuning range and provides a good phase noise of -120dBc/Hz at 1 MHz offset. The performance outcomes validate the effectiveness of the topologies and methodologies used in the design.

## ACKNOWLEDGEMENTS

The authors wish to thank the Ministry of Information and Communication Technology for the facilities provided in the laboratory of the Electronics& Instrumentation Engineering Department of SGSITS Indore under the SMDP-C2SD VLSI project.

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## AUTHORS PROFILES

**Mr. R.C. Gurjar** is currently working as an assistant professor in the Electronics & Instrumentation Engineering Department of Shri Govindram Seksaria Institute of Technology and Science Indore, M.P., INDIA since 2007. Mr.Gurjar received his Master of Engineering from Shri Govindram Seksaria Institute of Technology and Science Indore. he is currently pursuing his Ph.D. and his research areas are RFIC Design, Embedded System Design.

**Dr.D.K.Mishra** is currently working as a professor in Electtonics & Instrumentain Engineering Department of Shri Govindram Seksaria Institute of Technology and Science Indore since 1998. Dr Mishra received his Ph.D. and PG from SGSITS Indore. His research areas are RFIC Design and design of ADC/DACs.