

Low Power Fin Field Effect Transistor Based Combinational Circuits Design Using Gate Diffusion Input Method

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ABSTRACT

The electronic market is growing very rapidly because most of the devices are compact, innovative, efficient and consumes less power. Because of superiority in the semiconductor technology, integration of the whole electronics system on a single chip is in effect. The conventional CMOS has a Short Channel Effect. In order to reduce the Short Channel Effect, FinFET (Fin Field Effect Transistor) is used. It is the new emerging transistor that can work in the nanometer range to overcome these Short Channel Effects. Gate Diffusion Input (GDI) is used to reduce the power consumption of digital circuits. FinFET based digital circuits such as Full Adder, Full Subtractor, 2:1 MUX and 4:1 MUX are designed by using GDI technique. The Short Gate (SG) mode is used here. The technology used is 20nm at HSPICE software.

Keywords: FinFET, Full Adder, Full Subtractor, GDI, MUX, Short Channel Effect.

1. INTRODUCTION

Due to the development of technology, it has become essential to have a chip that requires minimum power, less power delay with efficient output. The improved digital circuits are designed in terms of less number of transistors, delay, average power, power delay product. The GDI (gate diffusion input) technique using FinFET has its own advantages. The full adder, full subtractor and MUX are the basic blocks of an FPGA and ALU unit. Hence it is designed with less number of transistors and less delay compare with the conventional combinational circuits.

Moore's Law refers to Moore's perception that the number of transistors on a microchip twice every two years, though the cost of a computer is reduced by 50%. Due to the increase in complexity on a chip the area and power consumption of the chip get increases. As power consumption increases, the temperature on the device increases, which further changes the characteristics of the device. FinFET technology provides the high drive current for a given transistor footprint, resulting in high speed, low leakage current, and low power consumption. The GDI method [1] allows reducing power consumption, propagation delay, and area of the digital circuit.

FinFET is a Fin Field Effect Transistor device structure. A FinFET is fabricated in a silicon layer overlying an insulating layer, and the device, prolong from an insulating layer as a fin. To provide enhanced drive current and effectively control short channel effects. Double gates are provided over the sides of the channel in FinFET.

FinFET is able to configure the back gate to grant greater speed and greater leakage control gives the goal for the designers to use FinFET to have a low power delay product.

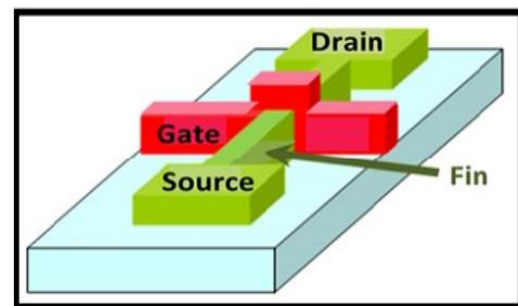


Fig.1 Double gate FinFET

1.1 MODES OF OPERATION

There are 4 types of operation modes in FinFET [2]. They are,

- Short gate (SG) mode
- Independent gate (IG) mode
- Low power (LP) mode
- IG/LP mode.

1.1.1 The Short-gate (SG) mode

In this mode of operation, both p-type FinFET and n-type FinFET are connected together. Fig.2 shows a NAND gate using the shorted gate mode. This configuration is best suited for high-performance applications.

Advantages

- Fastest under all load conditions

1.1.2 The Independent gate (IG) mode

In this mode of operation, the two gates are electrically independent and provide two different active modes of

operation with significantly different current characteristics determined by the bias conditions, the NAND gate schematic in IG mode shown in Fig.3.

Advantages

- Very low leakage
- Low switched capacitance

1.1.3 The Low power (LP) mode

In this mode of operation, the back gate is tied to reverse bias voltage to reduce leakage power, the NAND gate in LP mode is shown in Fig.4.

Advantages

- Low area and switched capacitance.

1.1.4 The hybrid (IG/LP) mode

This mode is a combination of LP and IG modes, NAND gate schematic for hybrid mode is shown in Fig.5.

Advantages

- Low leakage
- Low Area and switched capacitance

For example, the NAND gate schematic diagram for all 4 different modes is given below.

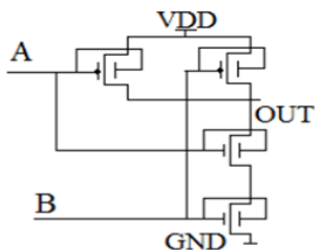


Fig.2 SG mode NAND gate

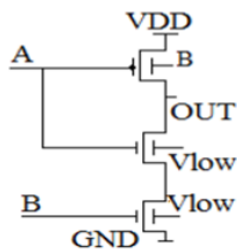


Fig.3 IG mode NAND gate

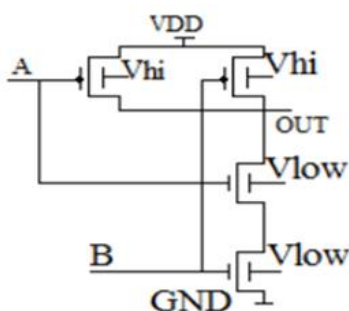


Fig.4 LP mode NAND gate

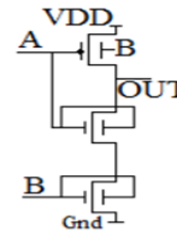


Fig.5 Hybrid (LP/IG) mode

In this section brief discussion on a Short Gate (SG) mode to design a digital circuit in FinFET is done. As it provides faster operation and works under all load conditions.

1.2 GDI TECHNIQUE

The Gate Diffusion Input (GDI) is an approach of low power digital combinatorial circuit design. It will reduce power consumption, propagation delay, and area of digital circuits while maintaining the low complexity of the logic design.

The GDI cell has three inputs. G -common gate input of NMOS and PMOS, P-input to the Source or Drain of PMOS, and N -input to the Source or Drain of NMOS. Bulks of both NMOS and PMOS transistors are connected to the N or P. So it can be arbitrarily biased, and in contrast with a CMOS inverter.

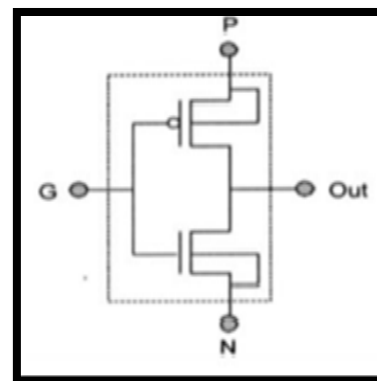


Fig.6 Basic GDI Cell

A GDI cell with four ports will be permitted as an alternate multi-functional device, which may promote six functions with quietly different combinations of input G, P and N.

2. WORKING OF FULL ADDER

A basic 1-bit Full Adder has three 1-bit inputs (A, B and C) and two 1-bit outputs (Sum and Carry). The output equations for the SUM and CARRY are given as follows:

$$SUM = A \text{ XOR } B \text{ XOR } C \quad \dots (1)$$

$$CARRY = (A (A \text{ XNOR } B)) + (C_{in} (A \text{ XOR } B)) = (B (A \text{ XNOR } B)) + (C_{in} (A \text{ XOR } B)) \quad \dots (2)$$

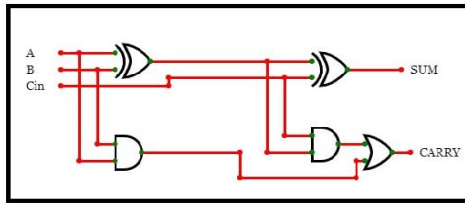


Fig.7 Logic diagram for Full Adder

Table.1 Truth Table for Full Adder

INPUT			OUTPUT	
A	B	C _{in}	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sum and Carry are implemented through the conventional CMOS Full Adder using 28 transistors [3]. This consists of PMOS pull-up and NMOS pull-down network. The major drawback of conventional CMOS is that utilizes a large number of transistors and chip area.

2.1 PROPOSED DESIGN

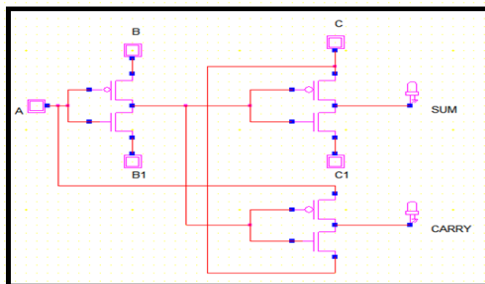


Fig.8 Proposed Full Adder circuit

This proposed GDI based, full adder circuit consists of only 6 transistors. When compared to the previously proposed 10T Full Adder [4], the number of transistors is reduced by 4. The proposed Full Adder circuit is designed by combining two XOR gates and one multiplexer. The inputs are A, B, B1, C, and C1, here B1 is the complement of B and C1 is the complement of C. The outputs are the sum and carry. The output of the sum is carried by two XOR gates.

$$SUM = A \text{ XOR } B \text{ XOR } C$$

The output of CARRY is carried by 2:1 multiplexer as,

$$CARRY = (A \oplus B) A \cdot (A \oplus B)$$

3. WORKING OF FULL SUBTRACTOR

A Full Subtractor is a combinational circuit which performs a subtraction between three bits. A (minuend), B (subtrahend) and C (borrow in). DIFF (DIFFERENCE) and BORROW are the outputs of Full Subtractor.

$$D = A'B'B_{in} + AB'B_{in}' + A'BB_{in}' + ABB_{in} \quad \dots (3)$$

$$B = A'B_{in} + A'B + BB_{in} \quad \dots (4)$$

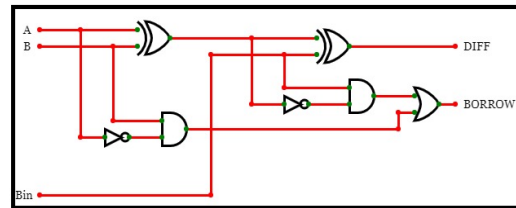


Fig.9 Logic diagram for Full Subtractor

Table.2 Truth Table for Full Subtractor

INPUT			OUTPUT	
A	B	C _{in}	DIFF	BORROW
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Full Subtractor architecture is implemented using 40T CMOS transistors [5]. This structure consists of a PMOS pull-up and an NMOS pull-down network. It includes the use of a large number of transistors, increased chip area. As a result, the propagation delay is high.

3.1 PROPOSED DESIGN

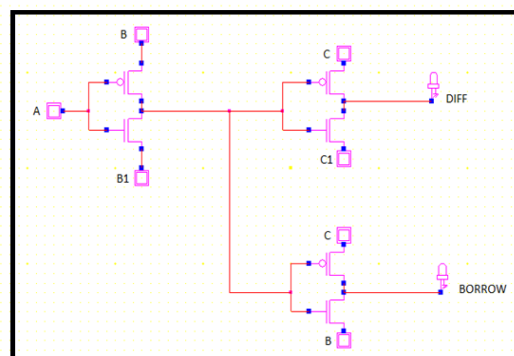


Fig.10 Proposed Full Subtractor

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In the proposed GDI architecture only 6 transistors are used to realize the operation of Full Subtractor. Whereas 14 transistors are used in the conventional method [6]. The number of transistors reduced by 8. The proposed Full Subtractor inputs are A, B, C, B1, and C1, where A1 is the complement of A, B1 is the complement of B and C1 is the complement of C. The outputs are DIFF and BORROW.
 $DIFF = A \oplus B \oplus C$

$BORROW = C.(A \oplus B) + \bar{A}.B$

GDI approach permits the implementation of an extension of complicated logic functions using only two transistors. This method produces a design which is fast with low power dissipation by using less number of transistors.

4. WORKING OF 2:1 MUX AND 4:1 MUX

A Multiplexer (MUX) is a device that gives much input into only one output.

$Y = (A. \bar{X}) + (B. X)$... (5)

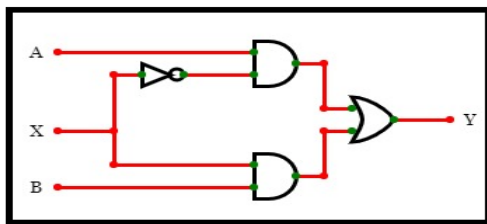


Fig.11 Logic diagram of 2:1 MUX

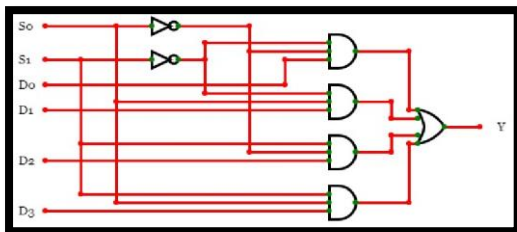


Fig.12 Logic diagram of 4:1 MUX

Table.3 Truth Table for 2:1 MUX

SELECTION LINE (X)	DATA INPUT	DATA OUTPUT
0	A	A
1	B	B

Table.4 Truth Table for 4:1 MUX

SELECTION LINE		DATA INPUT	DATA OUTPUT
S0	S1		
0	0	D3	D3
0	1	D2	D2
1	0	D1	D1
1	1	D0	D0

The conventional CMOS based 2:1 Multiplexer (MUX) is using 12T [7]. A 2:1 MUX is having only one Selection line X and Two data inputs are A and B. The output of 2:1 MUX is Y. Based on the selection line the corresponding data input is transferred to the output. If the selection line is '0' output is 'A', and the selection line is '1' output is 'B'.

The conventional CMOS based 4:1 Multiplexer (MUX) is using 46T [14]. A 4:1 MUX is having two selection line S0 and S1, and four data inputs D0, D1, D2 and D3. The output of 4:1 MUX is Y. Based on the selection line the particular data input only carried out.

4.1 PROPOSED DESIGN

This proposed GDI based 2:1 MUX circuit consists of the only 2T when compared to the previously proposed 12T 2:1 MUX [7]. The number of a transistor is reduced by 10. This circuit is having the inputs, namely X, A and B. The output is Y.

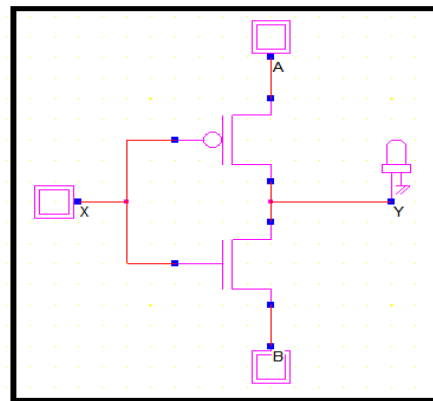


Fig.13 Proposed GDI method 2:1 MUX

This proposed GDI based 4:1 MUX circuit consists of the only 10T when compared to the previously proposed 46T 4:1 MUX [14]. The number of a transistor is reduced by 36. This circuit is having the inputs, namely S0, S1, D0, D1, D2 and D3. The output is OUT.

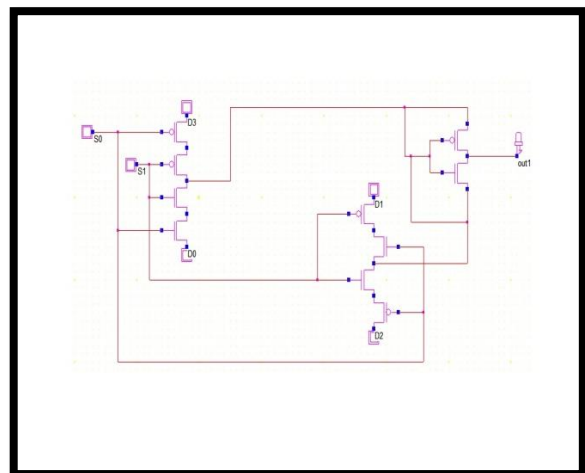


Fig.14 Proposed GDI method 4:1 MUX

5. DIFFERENT PARAMETERS

5.1.1 Dynamic power

When the device is actively switching from one state to another is called Dynamic power. The dynamic power consists of switching power consumed while charging and discharging the loads on a device, and internal power consumed internally to the device while it is changing state.

$$P_D = C_L V_{DD}^2 f_p \quad \dots (6)$$

5.1.2 Static power

It is the power consumed proceedings there is no circuit activity. For example, the power consumed by a D flip-flop when neither the clock nor the D input has active inputs. And the power consumed while the inputs are active.

$$P_S = I_{leakage} * V_{DD} \quad \dots (7)$$

Where P_S = Static power
 $I_{leakage}$ = Leakage current

5.1.3 Delay

Delay in VLSI system is the time between the trigger (change any signal level) on any pin or net of interest and the change in signal level of the same or other pin or net.

The time during the transition, when the output switches from 10% to 90% of the maximum value are called Rise time. The time during the transition, when the output switches from 90% to 10% of the maximum value are called Fall time.

$$Delay (\tau) = T(rf) + T(fr)/2 \quad \dots (8)$$

Where $T(rf)$ = time for rising to fall

$T(fr)$ = time for falling to rise

5.1.4 Leakage power

Leakage Power is defined as an undesirable sub-threshold current in the channel of a transistor when the transistor is turned off.

$$P = ACV^2 F_{CLK} \quad \dots (9)$$

Where P is the power consumed,

A is the activity factor of the circuit that is switching,

C is the switched capacitance,

V is the supply voltage,

and F is the clock frequency

6. SIMULATION RESULT

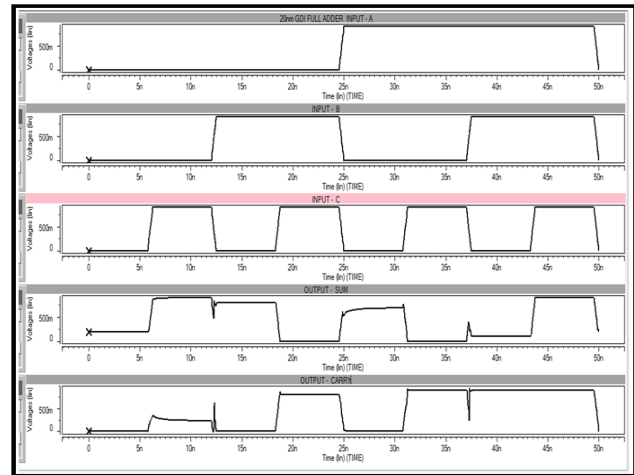


Fig.15 Output Waveform for Proposed Full Adder

Fig.15 Shows the Proposed Full Adder waveform. It consists of three inputs A, B, Cin. After adding these inputs the result will be carried out by SUM and CARRY. If the result without exists with CARRY, only SUM waveform part will be switched between '0' to '1' and '1' to '0'. Else the SUM and CARRY waveform part will be switched between '0' to '1' and '1' to '0'.

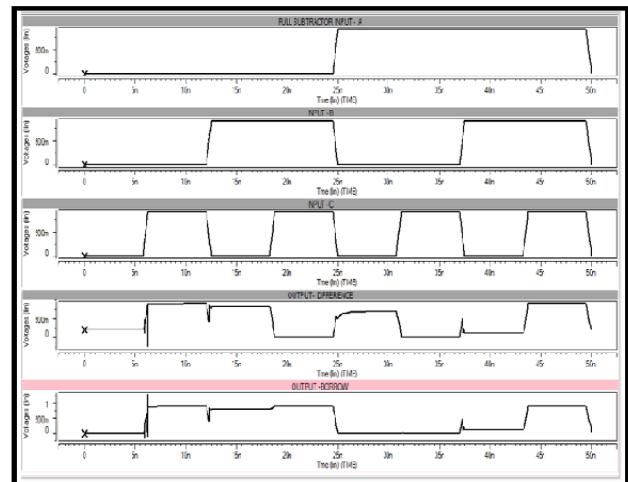


Fig.16 Output Waveform for Proposed Full Subtractor

Fig.16 Shows the Proposed Full Subtractor waveform. It consists of three inputs A, B, Cin. After subtracting these inputs the result will be carried out by DIFFERENCE (DIFF) and BORROW. If the inputs can be subtracted, only the DIFF waveform part will be switched between '0' and '1'. Else the DIFF and BORROW waveform part will be switched between '0' to '1' and '1' to '0'.

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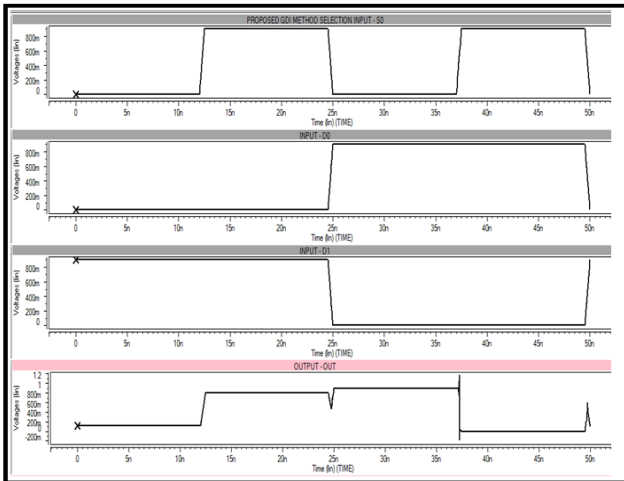


Fig.17 Output Waveform for Proposed 2:1 MUX

Fig.17 Shows the Proposed 2:1 MUX waveform. It consists of one selection line X, two data input A and B. Depending upon the selection line the corresponding data of A or B will be carried out by in the form of '0' or '1' through the OUT waveform part.

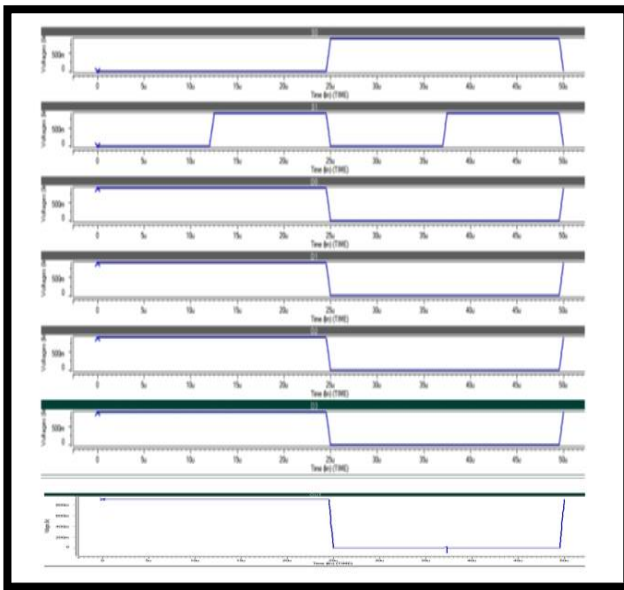


Fig. 18 Output Waveform for Proposed 4:1 MUX

Fig.18 Shows the Proposed 4:1 MUX waveform. It consists of two selection line S0, S1 and data inputs are D3, D2, D1 and D0. Based on the selection line the corresponding data will be transferred to the OUT waveform part.

Table.5 Comparison Table for Full Adder

Parameters	Conventional	IEEE (GDI)	Proposed (GDI)
No. of transistors used	28	10	6

Static power	2.91e-09	4.41e-09	1.97e-09
Dynamic power	2.56e-08	1.31e-08	4.24e-09
Delay	6.56e-09	6.34e-09	6.25e-08
PDP static	1.91e-17	2.80e-17	1.23e-17
PDP dynamic	1.68e-16	8.32e-17	2.64e-17

Table.5 shows the comparison of Full adder using conventional MOS transistor, IEEE GDI, and Proposed GDI is listed on there. Proposed GDI uses a less number of transistors to realize the Full adder operation. In the proposed method dynamic power consumption is reduced by 64% compared with conventional methods.

Table.6 Comparison Table for Full Subtractor

Parameters	Conventional	IJESC (GDI)	Proposed (GDI)
No.of transistors used	40	14	6
Static power	9.72e-09	4.30e-09	2.47e-09
Dynamic power	2.38e-08	7.93e-09	6.35e-09
Delay	6.24e-09	6.27e-09	6.26e-09
PDP static	6.07e-17	2.70e-17	1.55e-17
PDP dynamic	1.48e-16	4.97e-17	3.98e-17

Table.6 shows the comparison of Full subtractor using conventional CMOS transistor, IJESC (GDI), and Proposed GDI is listed on there. Proposed GDI uses a less number of transistors to realize the Full subtractor operation. In the proposed method dynamic power consumption is reduced by 25% compared with conventional methods.

Table.7 Comparison Table for 2:1 MUX

Parameters	Conventional	Proposed (GDI)
No.of transistors used	12	2
Static power	2.20e-09	3.43e-10
Dynamic power	5.46e-09	6.94e-10
Delay	1.27e-08	1.25e-08
PDP static	2.79e-17	4.30e-18
PDP dynamic	6.93e-17	8.72e-18

Table.7 shows the comparison of 2:1 MUX uses conventional MOS transistor, and Proposed GDI is listed on there. Proposed GDI uses a less number of transistors to realize the 2:1 MUX operation. In the proposed method dynamic power is reduced by 11% compared with conventional methods.

Table.8 Comparison Table for 4:1 MUX

Parameters	Conventional	Proposed
No.of transistors	46	10
Static Power	7.0529e-09	7.8912e-12
Dynamic Power	9.5634e-09	7.9669e-14
Delay	1.2491e-05	1.2500e-05
PDP Static	8.80977e-18	4.0836e-07
PDP Dynamic	1.19456e-13	5.5796e-08

Table.8 shows the comparison of 4:1 MUX using conventional CMOS transistor and Proposed GDI is listed on there. The Proposed GDI based 4:1 MUX circuit uses a less number of transistors. In the Proposed method, dynamic power consumption is reduced by 18% compared with conventional methods.

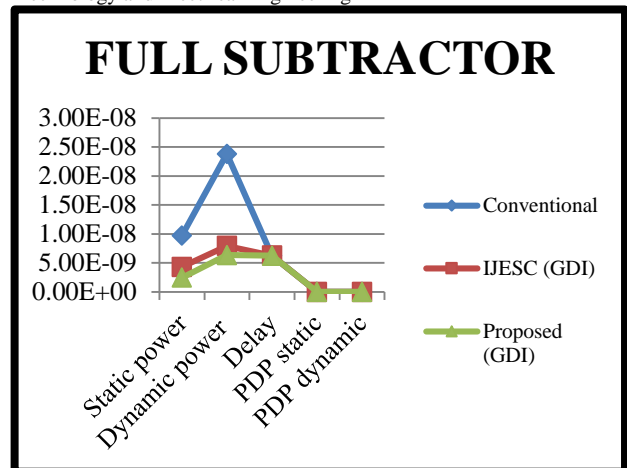


Fig.20 Comparison Chart for Full Subtractor

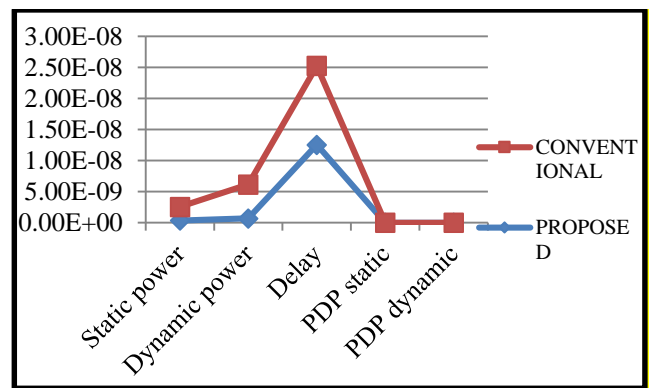


Fig.21 Comparison chart for 2:1 MUX

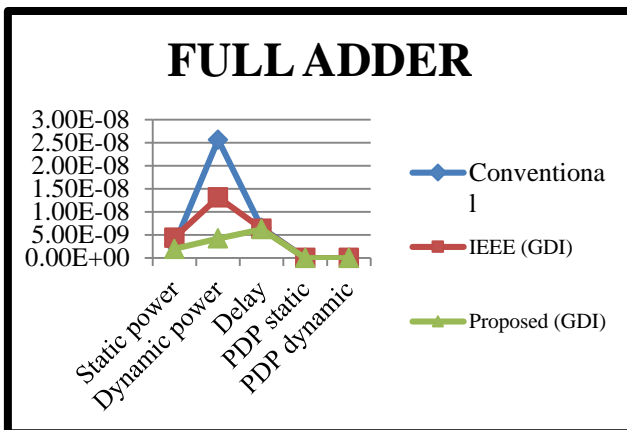


Fig.19 Comparison Chart for Full Adder

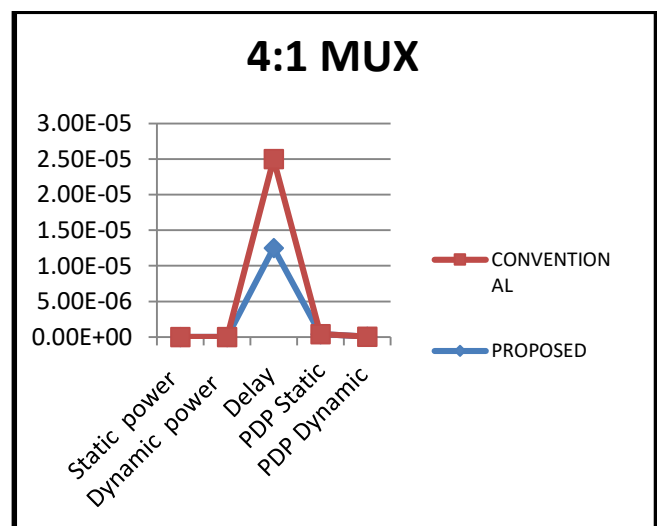


Fig.22 Comparison chart for 4:1 MUX

From these simulation results, the GDI based digital circuits are consumed less area, less power and less delay compared with conventional digital circuits.

7. CONCLUSION

An effective Gate Diffusion Input (GDI) technique is used in the proposed circuits to reduce the area by reducing the number of transistors used. It is apparent from the power consumption, that the GDI technique provides better performance than conventional techniques. And also it reduces the dynamic power, static power, delay, static power delay product, dynamic power delay product.

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