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A Novel Multi Level Inverter with Minimum Components and Maximum Switching Redundancy

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ABSTRACT

This paper presents a transformer-based multilevel inverter (MLI) topology, which reduces the overall cost of the system with lesser number of components than a conventional MLI. In this paper, a nine level MLI is designed which uses only eight switches, whereas a conventional transformer-less MLI requires 16 switches for achieving a nine-level voltage. The proposed structure consists of a single dc source feeding two standard H-bridges and a single transformer achieves the process of intermediate voltage regulation. Here, a pulse width modulation scheme is used to derive the gating pulses. In addition, only a single dc source is used for the MLI. The main advantage of this design is that several switching redundancies are possible for the various voltage levels. This decreases the switching losses. The proposed MLI is validated using MATLAB simulations. Also, an extension of the designed inverter to any higher number of voltage levels is also easily possible, and is shown.

Keywords: *Transformer based multi level inverter topology, pulse width modulation scheme, standard H-bridges.*

1. INTRODUCTION

Multilevel inverters (MLIs) include an array of power electronic devices whose output generate voltages with stepped waveforms. Inverters are power electronic devices, which converts dc power into ac power at a desired output voltage and frequency. The two level conventional inverter operates at high switching frequency, with high switching losses. It also faces harmonic distortion, EMI and high stress problems. So, it is difficult to interface these directly to high and medium voltage grids. Thus, there is a need for a different topology of inverters with multiple voltage levels.

Nowadays, MLIs are becoming more popular in power applications such as electric locomotives, renewable power generation etc. [1], as they have the ability to meet the increasing demand of power rating and power quality along with reduced harmonic distortion and lower electromagnetic interference. With higher number of voltage levels in the inverter, the power rating of the inverter can be increased and this reduces the device rating of the inverter. Inverters providing higher number of voltage levels are needed to cater the needs of versatile industrial applications such as, variable frequency drives in pumps & conveyors, HVDC transmission and UPS systems. Thus, the attractive features of MLIs can be summarised as follows:

- Higher number of voltage levels
- Reduced harmonic distortion
- Lower switching losses
- Fundamental and high switching frequency operation
- Staircase waveform quality
- Higher power quality
- Better electromagnetic compatibility

One main disadvantage of MLIs is the large number of power semiconductor switches needed, each of which have a related gate driver circuit that adds more complexity to the system. Thus the overall system cost will increase. So, recent researches are focused on reducing the complexity of the circuit by decreasing the number of power electronic switches and gate driver circuits.

MLIs can be broadly classified into transformer less and Transformer-Based MLIs (TBMLI). The first transformer less MLIs were capable of generating a three level voltage. Several different MLI topologies have emerged over the years [2]-[6]. The most significant among them being, the Diode-Clamped MLI, also known as the Neutral Point Clamped MLI (NPC), Cascaded-H-Bridge MLI (CHB), Flying capacitor MLI (FC), and their variants. All the above topologies have their unique characteristics, advantages and disadvantages. For a high-resolution output voltage, the CHB MLI requires a number of isolated dc sources. FC MLIs has an inherent voltage-unbalancing issue in the capacitor. In addition, they require a greater number of capacitors. Thus to eliminate these problems, many MLIs emerged, combining different conventional as well as non-conventional topologies. Nevertheless, most of these MLIs require a number of sensors and other components, thus adding on to the total cost of the MLI.

In this paper, a new nine-level transformer-based MLI with minimum number of components is designed. Two H-bridges that are fed from a single DC source shares the primary and secondary windings of the single-phase transformer. The proposal generates maximum switching redundancy for the various voltage levels. Furthermore, apart from the basic nine-level structure, a feasible method of extension of the proposal for an increased number of voltage levels is also given.

The rest of this paper is structured as follows: Section II summarizes the novel MLI Structure. Switching states and

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redundancies are explained in Section III. The various modes of operation of the MLI are described in Section IV. Calculation of transformer turns ratio is explained in Section V. In next section, a comparison of the novel MLI with other state of the art MLI topologies is done. Section VII gives the simulation results.

2. NOVEL MLI STRUCTURE

As shown in Fig. 1(a), the circuit diagram of the nine level transformer-based MLI consists of a single DC source, a single transformer and two standard H-bridges. To expand the novel MLI to obtain a higher number of voltage levels, additional H-bridges are added to the basic structure. The basic structure consists of primary winding connection of the injection transformer to the output of the front-end H-bridge, and the load connection across the output terminals of the back-end H-bridge which is in series with the secondary winding of the transformer. These H-bridges share the same input DC source, thus being economically advantageous. As represented in Fig. 1(b), the secondary of the injection transformers are cascaded to obtain the output voltage v_0.

The backend H-bridge consisting of the switches S_a, S_b, S_c, and S_d remains unchanged, even though any extra number of extra

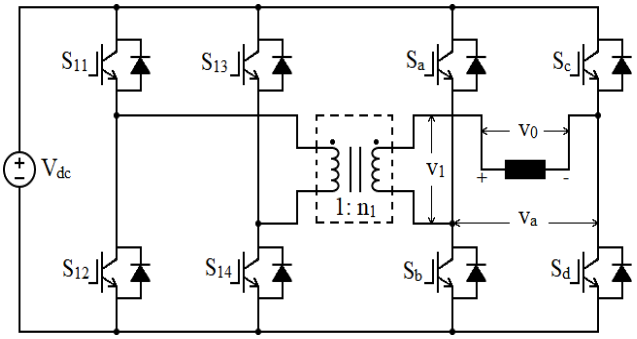

Fig.1 (a). Circuit diagram of the proposed MLI

H-bridge modules are added, and thus it is referred to as a Fixed CHB (FCHB). Unlike conventional CHB MLIs, the level generation in this proposed topology is achieved from the voltage across the secondary winding, thereby requiring lesser number of transformers and thus making the topology more economic than other similar topologies. The output voltage, V_a given by the FCHB is given as,

$$V_a = V_0 - V_1, \quad (1)$$

where V_0 represents the load voltage and V_1 is the secondary terminal voltage of the transformer. This voltage is equal to n_1 times the transformer input voltage. From (1), V_0 is given by,

$$V_0 = V_a + V_1, \quad (2)$$

So, the output voltage for the extended structure of the designed topology is as given below:

$$V_0 = V_1 + V_2 + V_3 + \ldots + V_{p-1} + V_p + V_a \quad (3)$$

where V_1, V_2,…, V_p represents the voltage across the secondaries of the transformers.

3. SWITCHING STATES AND REDUNDANCIES

The proposed transformer-based MLI topology produces a nine-level output voltage waveform by applying appropriate switching states. The topology also features maximum number of redundancy in switching states. That is, to produce the same output voltage level, there are more than one switching state combinations possible. Thus, these multiple redundancies add to the practicality of the proposed MLI. From the 16 switching states possible for the top four switches of the MLI, four switching redundancies are observed in the generation of zero voltage across the primary winding of the transformer, which is one among the three voltage levels that a standard H-bridge can produce. For example, zero voltage can be achieved by switching ON the top four switches and switching OFF the bottom four switches of the MLI structure and vice versa. Also, two switching redundancies each are obtained for the voltage levels + $V_{dc,}$ - $V_{dc,}$ + n_1 V_{dc} and - n_1 V_{dc}. That is, a maximum number of redundancies are obtained with a minimum number of switches for a nine level MLI.

Suitable switching states are selected out of the redundancies, so that fundamental switching of two switches out of eight are achieved over a full cycle. The relationships between the number of switches (S), the number of voltage levels (L), and the number of gate driver circuits (G), for a given number of transformers (T), for the extended structure configuration, are given as,

$$L = T + 1 \quad (4)$$

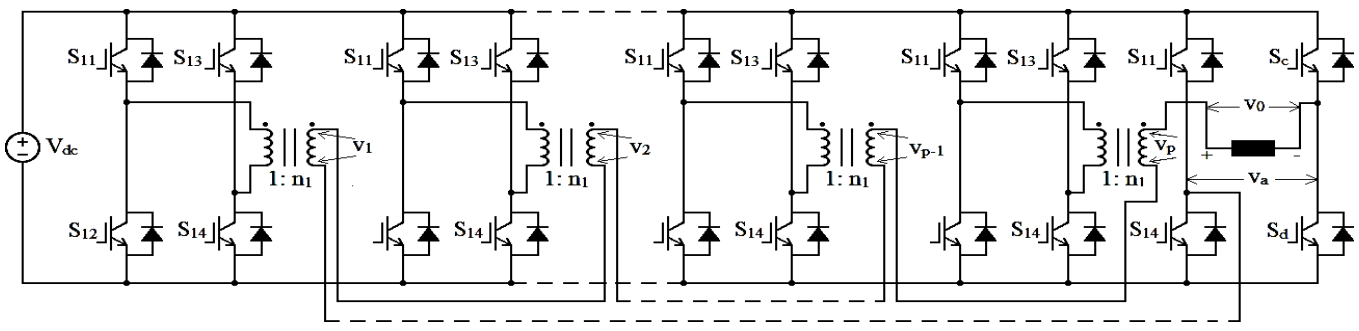

Fig.1 (b). Extended MLI Configuration

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$$S = G = 4\,(T + 1) \quad (5)$$

The switching states, (with the above described redundancies) for generating the nine-levels of the proposed transformer-based MLI is shown in Table I. The values "0" and "1" corresponds to OFF-state and ON-state of the switches respectively, for a given level.

Table- I: 16 switching states of the proposed MLI along with the redundancies

S_{11}	S_{13}	S_a	S_c	V_1	V_a	V_0
0	0	0	0	0	0	0
1	1	1	1	0	0	0
0	0	1	1	0	0	0
1	1	0	0	0	0	0
1	1	1	0	0	$+V_{dc}$	$+V_{dc}$
0	0	1	0	0	$+V_{dc}$	$+V_{dc}$
1	0	0	1	$+n_1V_{dc}$	$-V_{dc}$	$+(n_1\text{-}1)Vdc$
1	0	0	0	$+n_1V_{dc}$	0	$+n_1V_{dc}$
1	0	1	1	$+n_1V_{dc}$	0	$+n_1V_{dc}$
1	0	1	0	$+n_1V_{dc}$	$+V_{dc}$	$+(n_1+1)Vdc$
0	0	0	1	0	0	$-V_{dc}$
1	1	0	1	0	$-V_{dc}$	$-V_{dc}$
0	1	1	0	$-n_1V_{dc}$	$+V_{dc}$	$-(n_1\text{-}1)Vdc$
0	1	0	0	$-n_1V_{dc}$	0	$-n_1V_{dc}$
0	1	1	1	$-n_1V_{dc}$	0	$-n_1V_{dc}$
0	1	0	1	$-n_1V_{dc}$	$-V_{dc}$	$-(n_1+1)Vdc$

4. MODES OF OPERATION

Modes of operation for the positive and negative half cycles of the output voltage are described below in detail. The dashed lines in the circuit diagrams that follow, represents sections that does not allow the flow of current. Modes of operation for the positive half cycle is as shown below:

A. Mode 0

In Mode 0, a zero level of voltage is generated across the load. From the 16 switching states shown in Table-I, zero voltage can be obtained from four switching redundancies. One of the possible switching states for zero voltage level is shown in the Fig. 2 (a); when switches S_{12}, S_{14}, S_b, and S_d are ON, and the other four (S_{11}, S_{13}, S_a, and S_c) of them are OFF, resulting in, $V_1 = 0$, and $V_a = 0$. Therefore, from (2), output voltage across load, V_0 is zero.

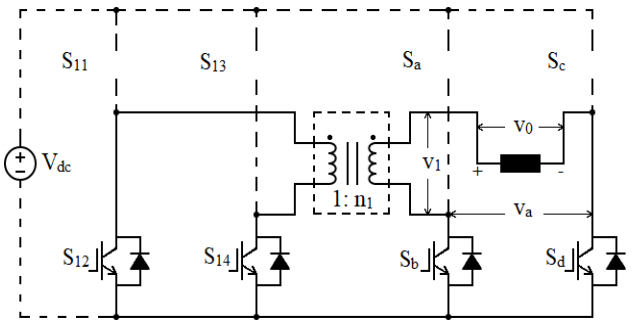

Fig. 2 (a) Mode 0

B. Mode 1

In Mode 1, $+V_{dc}$ level of voltage is generated across the load. From the 16 switching states shown in Table-I, $+V_{dc}$ voltage can be obtained from two switching redundancies. One of the possible switching states for $+V_{dc}$ voltage level is shown in the Fig. 2 (b); when switches S_{12}, S_{14}, S_a, and S_d are ON, and the other four (S_{11}, S_{13}, S_b, and S_c) of them are OFF, resulting in, $V_1 = 0$, and $V_a = +V_{dc}$. Therefore, from (2), output voltage across load, V_0 is $+V_{dc}$.

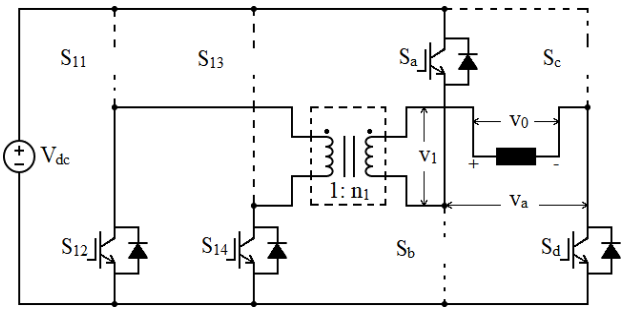

Fig. 2 (b) Mode 1

C. Mode 2

In Mode 2, $+(n_1\text{-}1)Vdc$ level of voltage is generated across the load. From the 16 switching states shown in Table-I, $+(n_1\text{-}1)Vdc$ voltage can be obtained from one switching combination. In Fig. 2 (c); when switches S_{11}, S_{14}, S_b, and S_c are ON, and the other four (S_{12}, S_{13}, S_a, and S_d) of them are OFF, resulting in, $V_1 = +n_1V_{dc}$, and $V_a = -V_{dc}$. Therefore, from (2), output voltage across load, V_0 is $+(n_1\text{-}1)V_{dc}$.

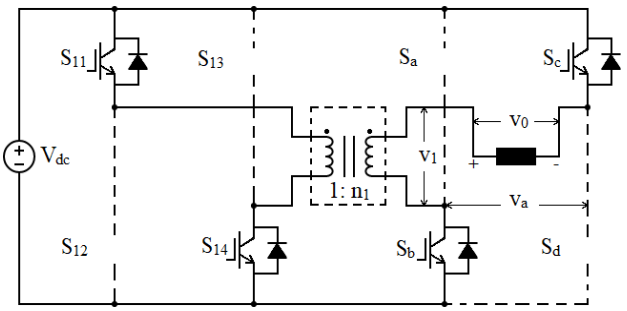

Fig. 2 (c) Mode 2

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D. Mode 3

In Mode 3, $+n_1V_{dc}$ level of voltage is generated across the load. From the 16 switching states shown in Table-I, $+n_1V_{dc}$ voltage can be obtained from two switching redundancies. One of the possible switching states for $+n_1V_{dc}$ voltage level is shown in the Fig. 2 (d); when switches S_{11}, S_{14}, S_b, and S_d are ON, and the other four (S_{12}, S_{13}, S_a, and S_c) of them are OFF, resulting in, $V_1 = +n_1V_{dc}$, and $V_a = 0$ as shown in the Fig. 2(d). From (2), V_0 is $+n_1V_{dc}$.

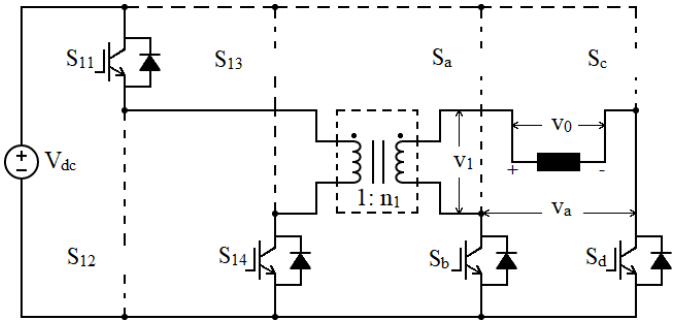

Fig. 2 (d) Mode 3

E. Mode 4

In Mode 4, $+(n_1+1)Vdc$ level of voltage is generated across the load. From the 16 switching states shown in Table-I, $+(n_1+1)Vdc$ voltage can be obtained from one switching combination. In Fig. 2 (e); when switches S_{11}, S_{14}, S_a, and S_d are ON, and the other four (S_{12}, S_{13}, S_b, and S_c) of them are OFF, resulting in, $V_1 = +n_1V_{dc}$, and $V_a = +V_{dc}$ as shown in the Fig. 2(e). From (2), V_0 is $+(n_1 + 1)V_{dc}$.

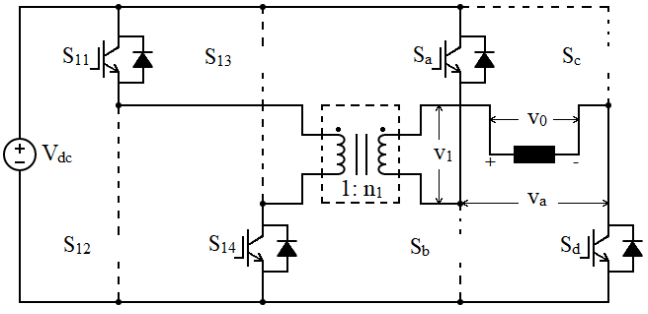

Fig. 2 (e) Mode 4

Modes of operation for the negative half cycle is obtained similarly as shown below:

A. Mode 0

In Mode 0, a zero level of voltage is generated across the load. From the 16 switching states shown in Table-I, zero voltage can be obtained from four switching redundancies. One of the possible switching states for zero voltage level is shown in the Fig. 3 (a); when switches S_{11}, S_{13}, S_a, and S_c are ON, and the other four (S_{12}, S_{14}, S_b, and S_d) of them are OFF, resulting in, $V_1 = 0$, and $V_a = 0$. Therefore, from (2), output voltage across load, V_0 is zero.

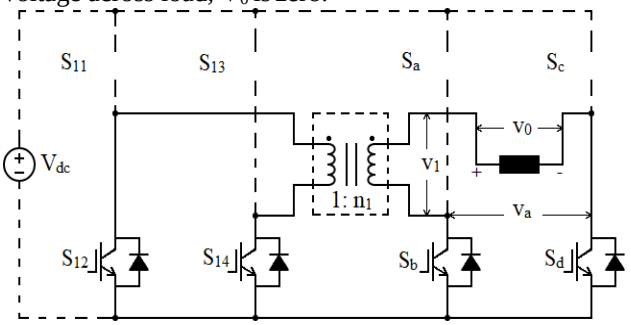

Fig. 3 (a) Mode 0

B. Mode 1

In Mode 1, $-V_{dc}$ level of voltage is generated across the load. From the 16 switching states shown in Table-I, $-V_{dc}$ voltage can be obtained from two switching redundancies. One of the possible switching states for $-V_{dc}$ voltage level is shown in the Fig. 3 (b); when switches S_{11}, S_{13}, S_b and S_c are ON, and the other four (S_{12}, S_{14}, S_a, and S_d) of them are OFF, resulting in, $V_1 = 0$, and $V_a = -V_{dc}$. Therefore, from (2), output voltage across load, V_0 is $-V_{dc}$.

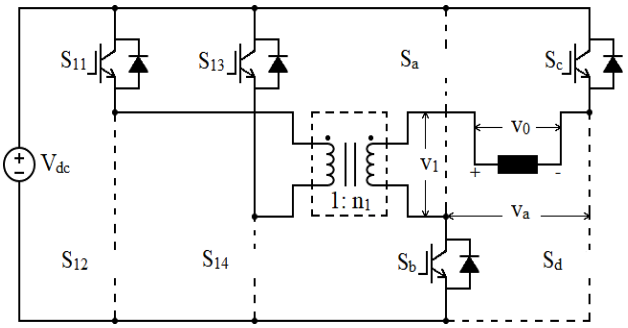

Fig. 3 (b) Mode 1

C. Mode 2

In Mode 2, $-(n_1-1)Vdc$ level of voltage is generated across the load. From the 16 switching states shown in Table-I, $-(n_1-1)Vdc$ voltage can be obtained from one switching combination. In Fig. 3 (c); when switches S_{13}, S_{12}, S_a and S_d are ON, and the other four (S_{11}, S_{14}, S_b, and S_c) of them are OFF, resulting in, $V_1 = -n_1V_{dc}$, and $V_a = +V_{dc}$. Therefore, from (2), output voltage across load, V_0 is $-(n_1-1)V_{dc}$.

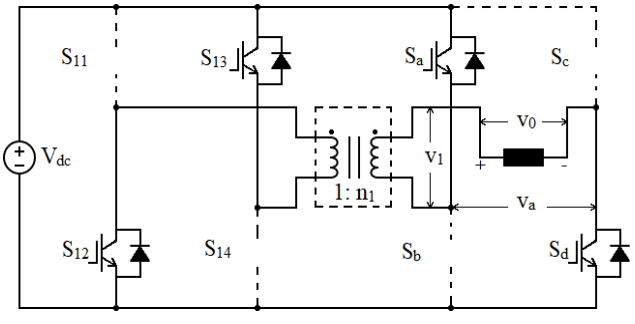

Fig. 3 (c) Mode 2

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D. Mode 3

In Mode 3, $-n_1V_{dc}$ level of voltage is generated across the load. From the 16 switching states shown in Table-I, $-n_1V_{dc}$ voltage can be obtained from two switching redundancies. One of the possible switching states for $-n_1V_{dc}$ voltage level is shown in the Fig. 3 (d); when switches S_{13}, S_{12}, S_a, and S_c are ON, and the other four (S_{11}, S_{14}, S_b, and S_d) of them are OFF, resulting in, $V_1 = -n_1V_{dc}$, and $V_a = 0$ as shown in the Fig. 2(d). From (2), V_0 is $-n_1V_{dc}$.

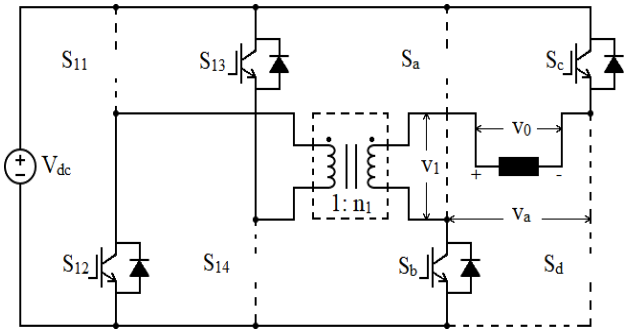

Fig. 3 (e) Mode 3

E. Mode 4

In Mode 4, $-(n_1+1)Vdc$ level of voltage is generated across the load. From the 16 switching states shown in Table-I, $-(n_1+1)Vdc$ voltage can be obtained from one switching combination. In Fig. 3 (e); when switches S_{13}, S_{12}, S_b, and S_c are ON, and the other four (S_{11}, S_{14}, S_a, and S_d) of them are OFF, resulting in, $V_1 = -n_1V_{dc}$, and $V_a = -V_{dc}$ as shown in the Fig. 2(e). From (2), V_0 is $-(n_1+1)V_{dc}$.

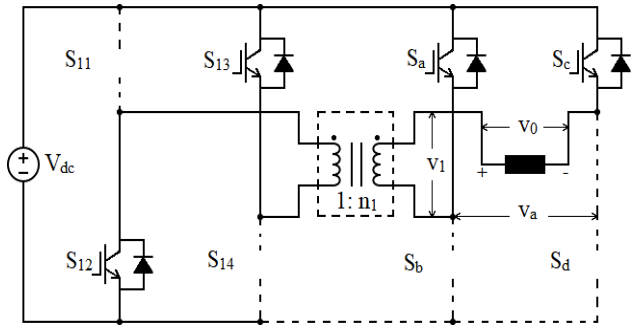

Fig. 3 (e) Mode 4

5. CALCULATION OF TRANSFORMER TURNS RATIO

The number of output voltage levels of this inverter mostly depend on the transformer turns ratio (n_1). So, calculation of transformer turns ratio is a crucial step. n_1 must be chosen such that a maximum number of output levels are obtained and they are equally spaced. An equally spaced output voltage waveform is generated for $n_1 \leq 3$ in this paper. n_1 above this will result in an unequally spaced output waveform, even though the number of output levels will remain the same. $n_1>3$ will result in an output waveform with higher harmonic distortion and hence such a situation has to be avoided. This topology generates five, seven, and nine-level voltage waveforms respectively, for n_1 values of 1, 2 and 3. The transformer turns ratios of the multiple transformers that has to be used for an extended version of the designed MLI topology can be obtained using any one of the following methods:

- Method 1:

Here, the turns ratios of the consecutive transformers are chosen in such a way that their algebraic difference is same. Difference value between the transformers turns ratios is represented by r and is expressed as,

$$r = n_2 - n_1 = n_3 - n_2 = \ldots = n_p - n_{p-1} \quad (6)$$

The total number of output levels generated corresponds to $2(n_1+1)+1$, and the peak value of the output voltage corresponds to $(n_1+1)V_{dc}$ (using a single transformer). From (6), r = 1, 2, 3,…,r_{max} and for output voltage waveform with equally spaced steps, $r_{max} = n_1+3$.

The number of output levels N_L produced for a specific number of transformers T is given as,

$$L = 2\,Tn_1 + (T^2 - T)\,r + 3 \quad (7)$$

Thus a symmetric topology is obtained where n_1 is the transformers turns ratios when r = 0.

- Method 2:

Here, the transformer turns ratio of the any transformer is half that of the succeeding transformer, represented by the relation shown below.

$$n_2 = 2n_1,\ n_3 = 2n_2,\ldots,\ n_p = 2n_{p-1} \quad (8)$$

The expression relating the number of levels N_L and number of transformers N_t is represented as,

$$L = 2^{T+1}\,n_1 - 2n_1 + 3 \quad (9)$$

- Method 3:

Here, the transformer turns ratio of the any transformer is one-third that of the succeeding transformer, represented by the relation shown below.

$$n_2 = 3n_1 n_3 = 3n_2,\ldots,\ n_p = 3n_{p-1} \quad (10)$$

The expression relating the number of levels N_L and number of transformers N_t is represented as,

$$L = 3^T\,n_1 - n_1 + 3 \quad (11)$$

It is seen from the various methods mentioned above, that the maximum number of output voltage levels with equally spaced steps is produced when transformer turns ratio is $n_1 = 3$. Therefore, the transformer turns ratio is chosen as $n_1 = 3$. The relation between the number of switches (S), the number of gate drive circuits (G) and the number of transformers (T) required to obtain a maximum number output voltage levels (L) are represented as,

$$S = G = 4\frac{\ln(N_L)}{\ln(3)} \quad (12)$$

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$$T = \frac{\ln(N_L)}{\ln(3)} - 1 \quad (13)$$

6. COMPARISON WITH CONVENTIONAL MLI TOPOLOGIES

A basic comparison of the novel inverter with major conventional MLI topologies are done based on the typical number of components. It is shown in Table II.

Table- II: Comparison of novel inverter with conventional MLI topologies

Topology	NPC	FC	CHB	Novel
Power switches	2(n-1)	2(n-1)	2(n-1)	(n-1)
Clamping diodes	(n-1) *(n-2)	0	0	0
DC bus capacitors	(n-1)	(n-1)/2	(n-1)/2	0
Balancing capacitors	0	((n-1)* (n-2))/2	0	0

'n' here represents the number of output levels of the MLI. Comparison with conventional multilevel inverters can be performed based on the following criteria also:

- Cost estimation associated with power circuit
- Amplitude of harmonic components
- Number of semiconductor devices in each phase leg
- Number of balancing capacitors in each phase leg
- Number of Dc bus capacitors present
- Control complexity based on power switches and voltage unbalances
- Total Harmonic Distortion in the output voltage

To validate the theoretical proposal, the novel inverter is simulated using MATLAB/Simulink software and the results are analyzed. The simulation diagram of the same is as given in Fig. 4.

A. Simulation Parameters

The simulation parameters used are detailed below:

- Input Voltage, $V_{dc} = 15V$
- R-L Load with $R = 40\Omega$ and $L = 10\mu H$
- Reference Sine wave with,
  - Amplitude = 50
  - Bias = 50
  - Frequency = 50Hz
- Transformer with nominal power = 10000VA and frequency = 60Hz
  - For winding 1,
    - $V_1 (V_{RMS}) = 1$
    - $R_1 = 0.1\Omega$
    - $L_1 = 0.0000001H$
  - For winding 2,
    - $V_2 (V_{RMS}) = 3$
    - $R_2 = 0.1\Omega$
    - $L_2 = 0.0000001H$
- Magnetisation Resistance = 1 and Magnetisation Inductance = 10
- $1:n_1 = 1:3$

B. Simulated Outputs

The waveforms obtained from the simulation is analysed. The transformer secondary voltage is obtained with minimum noise and is shown in Fig. 5.

The nine level output voltage and current obtained with minimum noise are shown in Fig. 6 and Fig. 7 respectively.

The waveforms are found to be in close proximity to the expected output waveforms from the theoretical proposal.

7. SIMULATION RESULTS

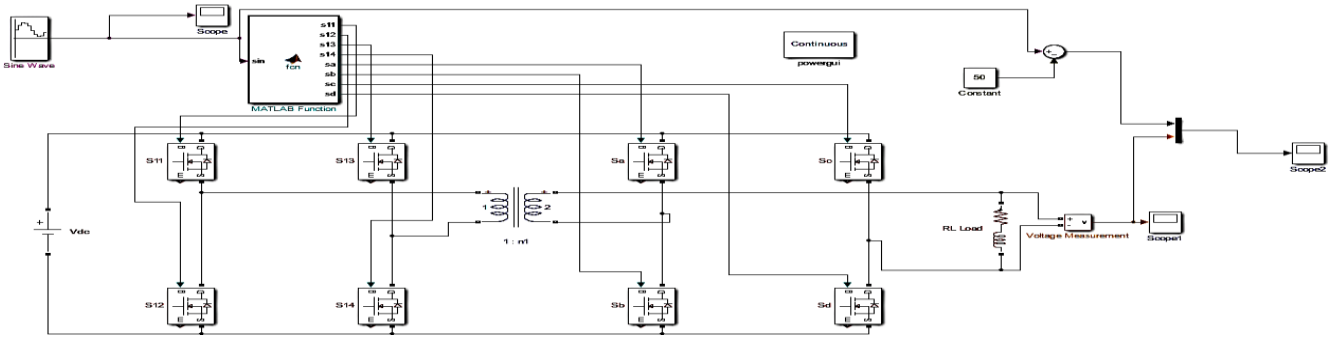

Fig. 4. Simulation diagram of the novel inverter

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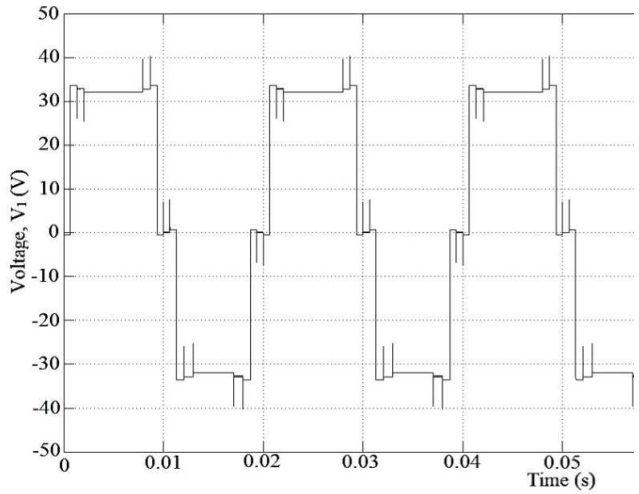

Fig. 5. Transformer secondary voltage

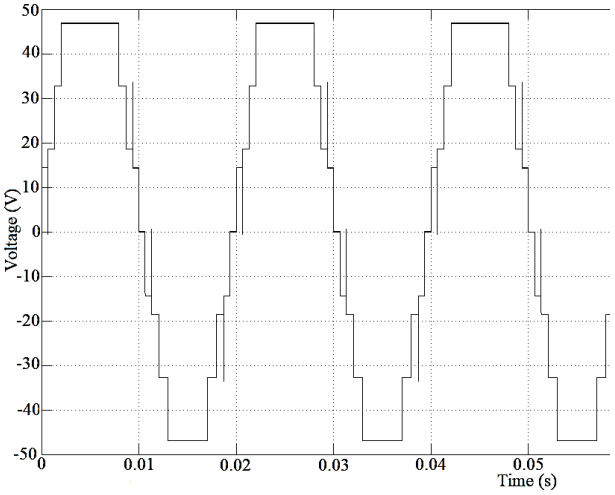

Fig 6. Nine level output voltage waveform

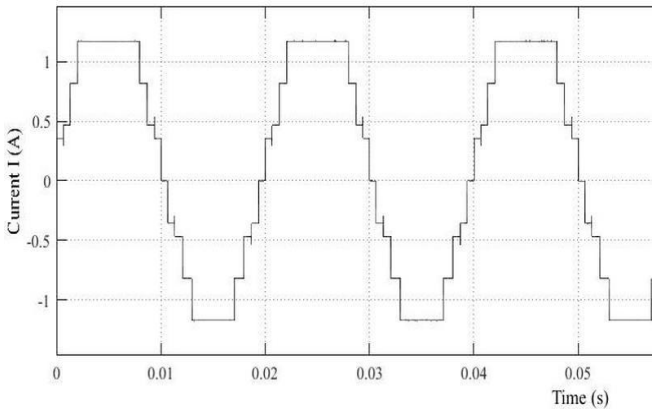

Fig. 6. Simulated current and voltage waveforms of the proposed converter

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