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Different Topologies of Low Noise Amplifier for Wideband Applications

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ABSTRACT

Low noise amplifier (LNA) is one of the important component of both RF transmitter and receiver. LNA amplifies very low power signal without producing any additional noise. As the demand for high speed data communication is increasing, the receiver requires large bandwidth and high sensitivity. LNA plays important role in such a wideband wireless communication system. The requirements of LNA are low NF, high gain over large bandwidth, low power consumption and compact chip area. This paper discusses the variation of these figure-of-merits (FOM) and different techniques used for LNA design in different works from the year 2013 to 2019.

Keywords*: IIP3, Impedance matching, Low noise amplifier, Noise figure, S-parameters, and Wideband*

1. INTRODUCTION

The demand for high speed wireless communication is increasing day by day. The radio waves are continuously attenuated by the environment and also additional noises are added to the signal. Therefore RF receiver requires a low noise amplifier to amplify this weak signal and to reduce the noise. As the first stage of RF receiver is the low noise amplifier, it should provide sufficient gain in order to reduce the noise in subsequent stages. High-frequency communication have large bandwidth than small frequency communication, which allows the higher-frequency transmission to send large amount of data in less time. For example a 5 GHz Wi-Fi system can carry more amount of data than a 2.5 GHz Wi-Fi system. In such situation, we need a wideband low noise amplifier that is operating in high frequency. But the design of a LNA is a challenging task in wideband communication, because it requires wideband input matching, very low power for battery backup, low noise figure for high signal to noise ratio (SNR), high gain and good stability. Since low noise amplifier is a two port network in RF environment S-parameter analysis is the better way for linear small signal analysis of low noise amplifier.

CMOS technology is one of the dominant technology used for the fabrication of RF integrated circuit due to its high level of integration that reduces the cost, low power consumption and high noise immunity. Continuous scaling down of CMOS technology enables the low noise amplifier to be designed on 0.13µm and 65nm CMOS technology. The design requirements and the typically acceptable values for a low nose amplifier are as follows,

Noise Figure	2dB
IIP3	-10dB
Gain	15dB
Impedance match	50Ω
Return loss	-15dB
Reverse isolation	20dB
Stability	>1

This paper focuses on the different topologies of low noise amplifier for wideband applications. The main contribution of this research is to give a comparison among different amplifier design techniques by stating limitations and future works in order to obtain a LNA with compact chip area. Section II contains different methods and techniques used year wise from 2013 to 2019 in LNA design for high gain and noise immunity. Section III contains, comparison of different methods for improving the performance of LNA.

3. RELATED WORK

Habib Rastegar et al. [1] designed a three stage low noise amplifier using source degeneration technique for UWB (Ultra-Wideband-Communication) applications. First stage is a cascode topology to achieve high gain and low noise figure. To improve the linearity a complementary push pull (CPP) topology is used. A common source (CS) is used at third stage to increase the gain. Wideband impedance matching is obtained through source inductive degeneration with high pass filter. To reduce the threshold voltage and power a forward body biased (FBB) technique was used. Fig.1 shows the proposed LNA circuit. The proposed LNA was stimulated in 0.13µm CMOS technology. The designed low noise amplifier achieves a gain of 19.5dB over entire bandwidth and a noise figure of 1-3.9dB.

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Yo-sheng Lin et al. [2] reported a two- stage inverter based LNA with three inductors in 0.18µm CMOS technology. Fig.2 shows the schematic diagram of the proposed LNA. Here a current reuse technique is used, i.e., dc current of M1 and M3

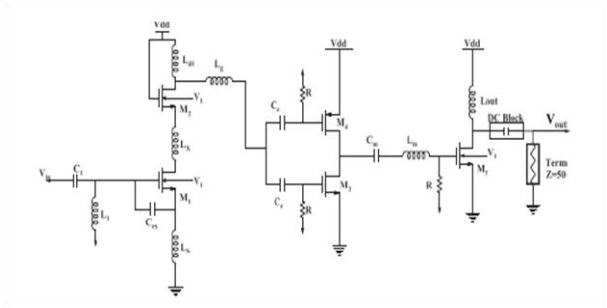

Fig. 1. Proposed LNA circuit [1]

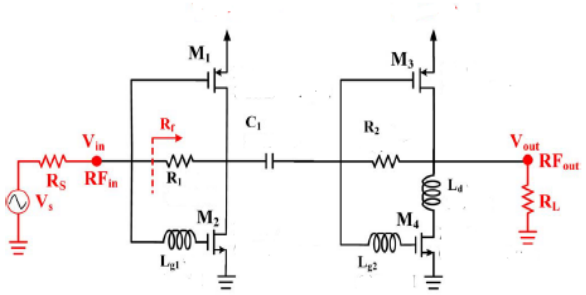

Fig. 2. Proposed LNA circuit diagram [2]

are reused by M2 and M4.Therefore no additional current is needed for M2 and M4.Wideband input impedance matching is achieved by enhanced π-match input network. This LNA achieves a flat and high gain over 3GHz-10GHz using gate inductors and parasitic capacitance. The designed LNA provides a gain of 11.5 dB over a bandwidth of 3-10GHz and a noise figure of 2.3dB. Even though high and flat gain is achieved, power consumption of 18 mW and chip area of 0.39 mm^2 is not satisfactory.

Li, Z et al. [3] proposed a new topology common Gate low noise figure with current-reuse technique and actives g_m boosting technique. Which can effectively restrain the power, enhance the gain and reduce the noise simultaneously. This method is able to reduce the power consumption under the condition of realizing input matching. It is implemented in 0.18µm CMOS technology. This LNA produce a 4.8dB noise figure and a gain of 14.7dB at 2.44GHz while consuming 0.58 mw from 1.8 V supply. Here also the chip area is very large.

Taeyoung Chung et al. [4] provide a wideband low noise amplifier that cancels IMD2 and IMD3.It uses a negative feedback to cancel thermal noise and non-linear harmonics.Fig.3 shows the circuit diagram of designed LNA. Here a large feedback resistor of 400Ω is used to reduce noise figure and a large transconductance is selected for first stage for impedance matching. The complementary CMOS parallel push-pull technique is used to cancel the IMD2.The IMD3 is cancelled by noise cancelling circuit. This is implemented in 65 nm CMOS technology, and provide a IIP3 of 5.5dBm.This technique give a power gain of 13dB and noise figure of 2.1-3.5dB in frequency range of 0.1 to 1.6GHz.

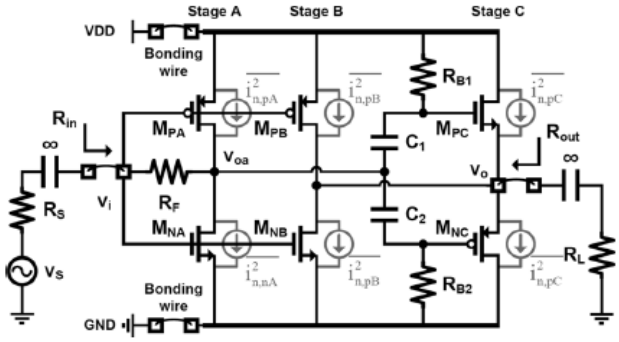

Fig. 3. Schematic of the designed LNA [4]

Wan, Q et al. [5] suggested a low power and high gain UWB LNA using a chartered 0.18µm CMOS process in the frequency range of 3.1 to10.6 GHz. Fig.4 shows the schematic of the proposed LNA. The LNA can achieve a wideband input matching and low NF simultaneously with resistive shunt feedback topology in congestion with the parallel LC load in the first stage. The modified current reused cascade configuration and forward body bias technique in the second stage reduce the power consumption while maintaining high gain and high reverse isolation. It provide high power gain, good input and output matching and excellent noise performance. It achieves a noise figure of 2.2-3.2dB while dissipating 9mW under a supply voltage of 1.5V. This technique has the disadvantage of large chip area and high power consumption.

Mahdi Parvizi et al. [6] suggest a complementary current reuse and tunable active shunt- feedback through forward body biasing (FBB) technique.Fig.5 shows the circuit of suggested LNA. A tunable active shunt feedback is used for input matching, that reduces the input impedance by a factor of (1+A) which make use of lower g_m for transistors and hence power consumption is reduced. Current reuse technique is also used to reduce power consumption. Current reuse can be achieved by flipping the NMOS and PMOS transistors in order to reuse the current of the feedback transistor in one of the input stage transistors. FBB is used to reduce g_m of feedback transistor.The reported LNA is implemented in 0.13µm CMOS technology. The proposed LNA provide a gain of 12.3dB and 4.9dB minimum noise figure over a bandwidth of 0.1-2.2GHz.

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Zhijian Pan et al. [7]. Here a low power inductorless wideband low noise amplifier is designed. The combination of common gate (CG) and common source with shunt feedback topologies (SFB) provide a cross coupled push-pull structure to LNA that is used for g_m boosting and partial noise cancellation. A cascode transistor is used to reduce miller effect and also current directing structure to increase bandwidth and gain. Optimization of sizing and biasing is also proposed under the power constraint. This LNA is fabricated in a 65nm CMOS technology. It exhibit a voltage gain of 21.2dB and a noise figure of 2.8-4dB over the frequency range of 100MHz to 4.3GHz.

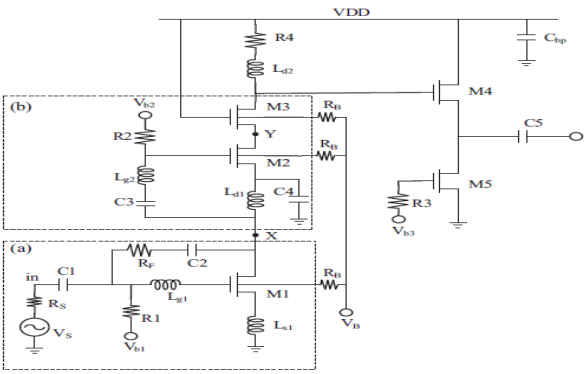

Fig. 4. Proposed circuit diagram [5]

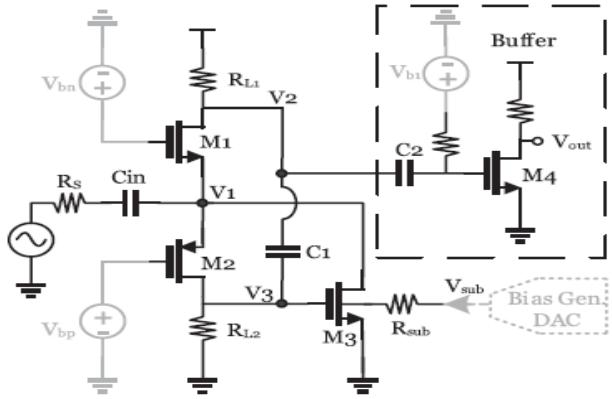

Fig.5. Schematic of the proposed LNA [6]

Pei Qin et al. [8] proposed a transformer based input matching network and transformer based gate-drain feedback is used to achieve gain and bandwidth extension based on source degeneration topology. In transformer based gate-drain feedback, the transformer is tied between gate and drain terminals of common gate transistor at output. The transformer based wideband input matching network improves input matching with compact size and cost. This network consists of a capacitor shunted at input and a transformer placed with its primary winding connected to gate and secondary winding shorted to ground. It provide a gain of 10.2dB and a bandwidth of 15.8 to 30.3GHz.It also provide a noise figure of 3.3dB.

S.Pandey et al. [9] proposed a compact wideband LNA for low power application.Fig.6 shows the circuit diagram of designed low noise amplifier. Here the common gate input stage exhibits improved radio frequency (RF) FOMs at reduced power supply. This common Gate topology provide better performance in terms of power gain and input matching. This is implemented in 0.18µm CMOS process. The proposed LNA consumes only 5.4mW power and .occupies a smaller chip area of $0.116mm^2$.Wideband input matching from 8.5 to 20GHz was obtained by using peaking inductors at the drain terminal of each stage. A low NF was obtained by selecting source degenerated inductors.

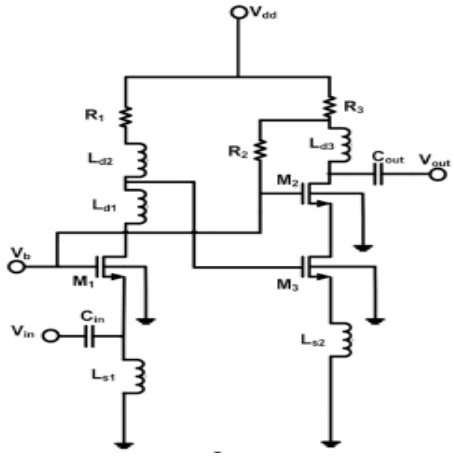

Fig.6. Proposed LNA [9]

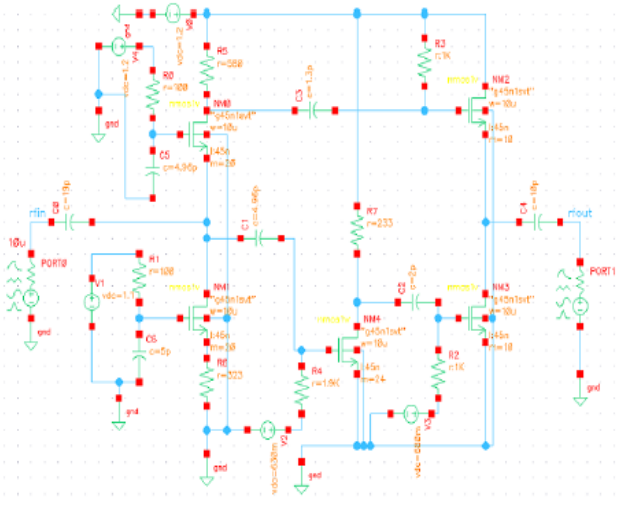

Fig.7. Schematic of the inductorless LNA [10]

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Mahesh Mudavath et al. [10] implemented an inductorless low noise amplifier with noise cancellation technique for portable receivers. Fig.7 shows the schematic of the inductorless LNA. The designed LNA contains common source (CS) and common gate (CG) amplifier stages. Input signal coming from source antenna with internal impedance R_S is fed to a matching of CS and CG amplifier. Noise cancellation technique is used to reduce the noise at the output of matching device. Principle of noise cancellation is based on the selection of two nodes in the circuit where the signal is appended with same polarity and the noise with opposite polarity, then if add these signals the noise is nullified. The perfect matching is achieved through common gate amplifier. It is implemented in CMOS 45nm GPDK technology. It provide a gain of 20dB over a bandwidth of 1.04-1.8GHz and a noise figure of 0.6-1.2dB.

3. COMPARISON

Table- II: Comparison of different methods

Ref.	[1]	[2]	[4]	[6]	[8]	[9]	[10]
Tech.	0.18µm	0.18µm	65nm	0.13µm	65nm	0.18µm	45nm
Gain, dB	9.5	11.5	13	12.3	10.2	11.13	20
BW, GHz	32	3-10	0.1-1.6	0.1-2.2	15.8-30.3	8.5-20	1.04-1.8
N, dB	4.1-7.6	2.3	2.1-3.5	4.9-6	3.3-5.7	2.1-3.2	0.6-1.2
Power, mW	71	18	20.8	0.4	12.4	5.4	7.8
S_{11},dB	< -10.5	<-10.7	< -8	-	< -10	< -9.44	< -11.2
S_{12},dB	< -10	-	-	-	-	< -26	< -55
IIP3,dBm	-	-0.2	5.5	-10	-0.5	0.96	-
Area,mm^2	0.58	0.39	0.014	0.052	0.18	0.116	-

4. CONCLUSION

From the review of wideband low noise amplifier we can see that they are mainly used in UWB, GSM, Wi-Max, WLAN, Satellite Communication and Mobile communication. In this paper we studied different LNA topologies proposed in various years to increase gain and to reduce noise figure over a large bandwidth. The low noise amplifiers are implemented using CMOS technology and its scaled version. A comparison of different methods showing variation in different parameters are also given. As a modification to this we will research on a compact low power wideband LNA with new topology. The work will focuses on increment of gain and decrement of noise figure for wideband wireless communication applications.

REFERENCES

[1] Rastegar, H., Saryazdi, S., Hakimi, A.: 'A low power and high linearity UWB low noise amplifier (LNA) for 3.1–10.6 GHz wireless applications in 0.13 µm CMOS process', *Microelectron. J.*, 2013, **44**, (3), pp. 201–209, ISSN 0026-2692.

[2] Yo-Sheng Lin, Chien-Chin Wang, Guan-Lin Lee, and Chih-Chung Chen,' High-Performance Wideband Low-Noise Amplifier Using Enhanced π -Match Input Network*', IEEE Microwave and Wireless Components Letters*, vol. 24, no. 3, March 2014.

[3] Li, Z., Wang, Z., Zhang, M., *et al.*: 'A 2.4 GHz ultra-low-power current-reuse CG-LNA with active g_m-boosting technique', *IEEE Microw. Wirel. Compon. Lett.*, 2014, **24**, (5), pp. 348–350

[4] Taeyoung Chung,Hankyu Lee, Daechul Jeong Jehyung Yoon and Bumman Kim,' A Wideband CMOS Noise-Canceling Low-Noise Amplifier With High Linearity', *IEEE Microwave and Wireless Components Letters*, May 24, 2015.

[5] Wan, Q., Wang, Q., Zheng, Z.: 'Design and analysis of a 3.1–10.6 GHz UWB low noise amplifier with forward body bias technique', *AEU-Int. J. Electron. Commun.*, 2015, **69**, (1), pp. 119–125.

[6] Mahdi Parvizi, Karim Allidina and Mourad N. El-Gamal, 'An Ultra-Low-Power Wideband Inductorless CMOS LNA With Tunable Active Shunt-Feedback*', IEEE Transactions on microwave theory and techniques*, April 16, 2016.

[7] Zhijian Pan, Chuan Qin, Zuochang Ye, Yan Wang, and Zhiping Yu,' Wideband Inductorless Low-Power LNAs

with G*m* Enhancement and Noise-Cancellation*'IEEE Transactions on circuits and systems–i: regular papers,* May 19, 2017.

[8] Pei Qin and Quan Xue,' Compact Wideband LNA With Gain and Input Matching Bandwidth Extensions by Transformer', *IEEE Microwave and Wireless Components Letters,* April 11, 2017.

[9] Sunil Pandey , Tushar Gawande, Shashank Inge, Abhijeet Pathak, Pravin N. Kondekar, 'Design and analysis of wideband low-power LNA for improved RF performance with compact chip area', *IET Microwaves, Antennas & Propagation*,2018.

[10] Mahesh Mudavath, K Hari Kishore, Sanjay Madupu, Prashanth Chittireddy , SrinivasBhukya,'Low Noise Amplifier Design of CMOS Inductorless with Noise Cancellation Technique', *International Journal of Engineering and Advanced Technology (IJEAT*) ISSN: 2249 – 8958, Volume-9 Issue-1, October 2019

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