Volume 9, Issue 3
June 2020

ITEE Journal
Information Technology & Electrical Engineering

ISSN: - 2306-708X

POWER FACTOR CORRECTED BLDC MOTOR DRIVE FOR LOW POWER APPLICATION

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ABSTRACT

Brushless direct current (BLDC) motors are getting much attention nowadays due to the increased popularity of electric vehicles providing smooth and environmental friendly transport. Controlling the speed of the BLDC motor accurately with minimum torque ripple is a challenging task. Further, when a BLDC motor fed from AC supply through a controlled rectifier, it must meet the international standards with regards to THD. Hence power factor correction is necessary. The power factor corrected (PFC) BLDC motor drives are used for low-power applications. This paper presents a bridgeless Power Factor Corrected buck-boost converter along with a voltage source inverter (VSI) to control the speed of BLDC motor. Power factor correction improves the power quality by enhancing the power factor, and it can be implemented using hysteresis control. Bridgeless topology reduces the number of power electronic devices; hence the conduction loss can be reduced. Pulse Width Modulation technique is utilized to vary the motor speed. A MATLAB simulation model and corresponding results of this drive are presented to showcase its performance.

Keywords: *Brushless Direct Current (BLDC) motor, Bridgeless Buck-Boost Converter (BLBBC), Diode Bridge Rectifier(DBR), Power Factor Corrected (PFC), Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), Voltage Source Converter (VSC), Total Harmonic Distortion (THD).*

1. INTRODUCTION

Brushless DC motors are used in low power, household applications due to the features of high efficiency, low maintenance, high flux density per unit volume and low EMI problems. The other applications of BLDC motor include; transportation, in portable tools, motion control, HVAC, and in industrial tools, etc [1]. A BLDC motor is nothing but a combination of a controller and an AC motor. Input to the controller is always a DC supply. The controller converts this DC voltage into pulsating or rectangular 2-phase or 3-phase AC, fed to motor electromagnets and thereby stator fields get energized. The polarity of stator field changes in a sequential manner causes rotation of the stator field. The rotor permanent magnet follows the stator field due to the magnetic lock. The motor starts to run as a synchronous motor, hence the name DC synchronous motor. Also known as electronically commutated DC motor. For designing the power appliances, power quality issues are considering at first. According to the IEEE standards, THD must lay within 5% especially in household equipments [2]. When a BLDC motor is feeding through Diode Bridge Rectifier (DBR), the THD level increase up to 65%.Thus, the overall system power factor falls below 0.7 [3] . To avoid this limitation, a power factor corrected (PFC) converter is used in the input side of the converter to drive the motor. A comparison between different power factor corrected converters is presented in [4]. Continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are the two modes in which the PFC converter can operate. In CCM, inductor currents remain continuous, and it requires DC link voltage and supply voltage to be sensed. A PFC Buck-boost converter BLDC motor drive with a reduced sensor is presented in [5], a DBR followed by a buck-boost converter is used in this method. But the power electronic devices used in this method are more, hence the conduction loss is high. In this BLDC Motor Drive, Bridgeless buck-boost converter (BLBBC) is used, which avoids the usage of DBR. PFC bridgeless buck-boost converter fed BLDC motor is presented in [6]. However DCM operation results in more ripples in the output voltage and creates speed ripples in small motors. In this paper, the working of the converter is explained in section II. The control strategy of the overall scheme is presented in section III. The design of the passive component is an important procedure, which is explained in section IV. The simulation model and results are shown in section V.

2. BLDC MOTOR DRIVE

Fig.1 shows the circuit diagram of the proposed BLDC motor drive. The input ac supply is given to BLBBC. It converts input AC voltage into DC by making input current sinusoidal and also in phase with supply voltage to improve the power factor. A DC link capacitor (Cd) is connected in between BLBBC and voltage source converter (VSC).

A. Working of BLBBC

ITEE Journal
Information Technology & Electrical Engineering

ISSN: - 2306-708X

BLBBC used in the proposed BLDC motor drive operated under CCM. There are two modes of operation in each half-cycle. In positive half cycle switch Sp is controlled, diode D1, inductor Li1, diode Dp are used. Similarly, in negative half-cycle switch Sn is controlled, diode D2 inductor Li2 and Dn are used.

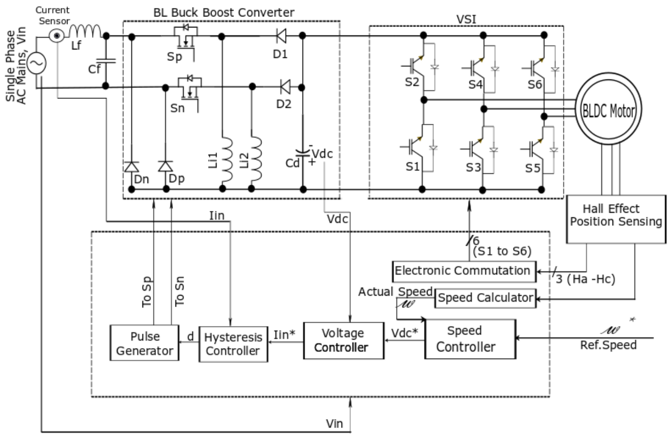


Fig.1. PFC BLDC motor drive.

Mode 1: Switch Sp/Sn is turned on, the voltage across inductor Li1/Li2 is now supply voltage and inductor current increases linearly through Dp/Dn. Energy stored in inductor increases, inductor current increases linearly. Fig.2 gives the current path during mode 1 operation.

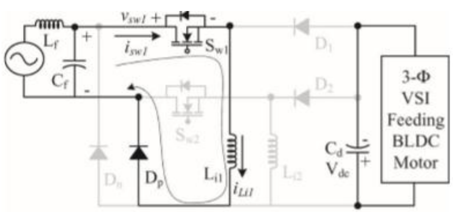


Fig. 2. Mode 1.

Mode 2: Switch Sp/Sn is turned off, the stored energy in inductor Li1/Li2 now de-energized to DC link capacitor and complete the path through diode D1/D2. Inductor current decreases and reaches zero. Fig.3 gives the current path during mode 2 operation.

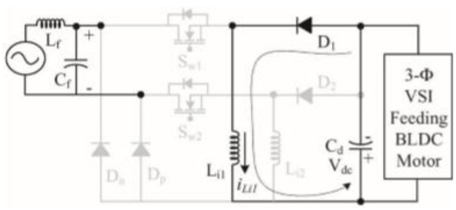


Fig. 3. Mode 2.

B. Working of VSC

VSC converter consists of 6 IGBTs, which are connected as shown in the fig.1. The gate pulse of IGBT is generated based on the Hall Effect signal of the BLDC motor. The switching pattern of IGBT according to Hall Effect input is shown in table 1. The switching frequency of IGBT is very low, hence the switching loss is low. For a 3 phase, BLDC motor each phase is connected to the middle of each leg. The top switch of a leg and bottom switch of another leg is turned on simultaneously. The voltage across two phases of BLDC motor is now connected across the DC link capacitor, whose voltage is equal to Vdc. The permanent magnet rotor now starts to rotate.

TABLE I
SWITCHING TABLE

Rotor angle (°)	Ha	Hb	Hc	Switches be turned on
NA	0	0	0	-
0-60	0	0	1	S1&S2
60-120	0	1	0	S2&S3
120-180	0	1	1	S3&S6
180-240	1	0	0	S4&S5
240-300	1	0	1	S4&S1
300-360	1	1	0	S2&S5
NA	1	1	1	-

Now Hall Effect sensors Ha, Hb, and Hc produce varying outputs for each 60º travel as shown in table 1. Consequently, the other two switches are turned on, and Vdc is now applied to different phases, which allows the rotor to rotate further.

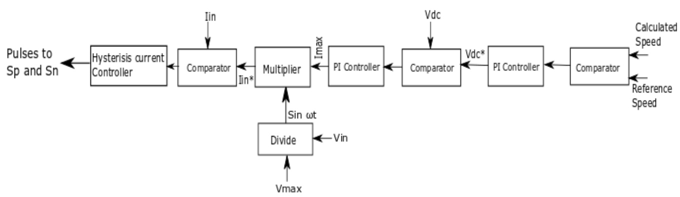


Fig. 4. Block diagram representation of Control.

The BLDC motor can be driven by successive switching as per the table 1.

2. CONTROL STRATEGY

In this paper, the hardware setup is same as shown in reference [6]. In reference [6], currents through inductor Li1 and Li2 are in DCM and hence it contains three modes of operation. In mode 1, inductor current increases linearly, which decreases to zero during mode 2. In mode 3, inductor currents remain at zero value and hence dc link capacitor, Cd discharges for a longer period. Therefore, this method results in increased voltage ripples and in turn creates speed ripples in

Volume 9, Issue 3
June 2020

ITEE Journal
Information Technology & Electrical Engineering

ISSN: - 2306-708X

BLDC motor. In this paper, hysteresis controller based control strategy is presented. Block diagram representation of control strategy is presented in fig.4. Here the actual speed is calculated from Ha, Hb, and Hc. Now the actual speed is compared with reference speed. The error signal is passed through a speed PI controller and reference dc Vdc* is obtained. Now, Vdc* is compared with actual Vdc and the error is passed through a voltage PI controller. This voltage controller generates Imax and is multiplied with the voltage wave shape obtained from input voltage sensor. So the multiplier generates current reference Iin*. Iin is measured using current sensor placed at the input side and both are given to hysteresis current controller to generate gate pulses. It is evident from fig.1, that only Sp is operated in positive half cycle and Sn is operated in negative half cycle of the supply voltage. Increased number of sensors are used here compared to reference [6]. However, low frequency (50Hz) sensors are used and are cheap and compact.

4. DESIGN

The PFC BL buck-boost converter is operated with hysteresis controller which spreads frequency over a range. Here the minimum switching frequency, f_{sw} is selected as 25kHz. The inductors are designed so that the current through it is in the boundary between CCM and DCM at f_{smin}. The rating of the selected BLDC motor is shown in table 2.

The power converter is designed to work at 500 W. The dc link voltage of the converter is designed for control from 80 V ($V_{dc\ min}$) to 250 V ($V_{dc\ max}$) with a typical value ($V_{dc\ nom}$) of 160 V; the duty ratios (d_{min} and d_{max}) corresponding to $V_{dc\ min}$ and $V_{dc\ max}$ are calculated as 0.2 and 0.55, respectively.

RMS value of supply voltage = 230 V

TABLE II
BLDC MOTOR RATINGS

PARAMETERS	VALUE
Rated Voltage	160 V
Rated Speed	3000 rpm
Power	500 W
No-load current	0.2 A

Average Voltage at input side = 207.07 V

A. Converter inductor design

The expression for critical inductance value of BL buck-boost PFC converter is given by the expression [6],

$$L_{ic1} = \frac{R(1-d)^2}{2f_{smin}} = \frac{V_{dc\,min}^2}{P_{min}}\frac{(1-d)^2}{2f_{smin}} \qquad (1)$$

From the above expression, the critical inductance value obtained as 800µH.

$$L_{i1} = L_{i2} = 800\mu H$$

B. DC link capacitor design

The expression for the DC link capacitor is given by

$$C_d = \frac{P_0/\,V_{dc\,nom}}{2\omega\Delta V_{dc}} \qquad (2)$$

Where ΔV_{dc} = 2% of $V_{dc\ nom}$, ω=2πf=100π, the DC link capacitance value is taken as 2200µF.

C. Input filters design

The required value of filter inductance is designed using the expression [6],

$$C_f = \frac{I_{peak}}{\omega V_{paek}} tan\theta \qquad (3)$$

Choosing θ = 1° , C_f is taken as 33 nF.

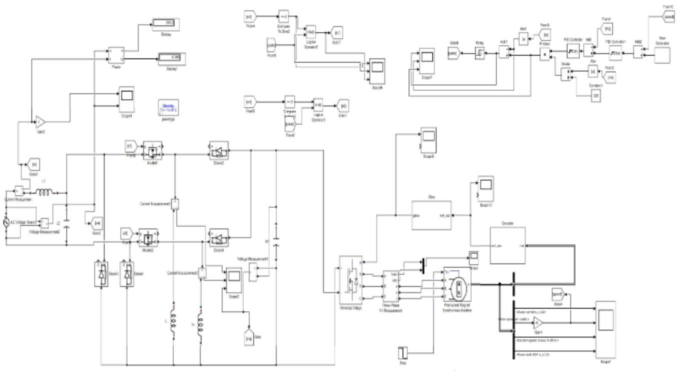
The required value of filter inductance is designed using the expression,

$$L_f = \frac{1}{4C_f(\pi f_{smin})^2} - 0.04\frac{1}{\omega L}\frac{V_S^2}{P_0} \qquad (4)$$

The calculated value for filter inductor is obtained as 7.16 mH.

5. SIMULATION RESULTS

Simulation of proposed BLDC motor drive is carried out in MATLAB Simulink. The Simulink model of the proposed converter is shown in fig.5. Input AC supply is given to BLBBC through an LC filter. A DC link capacitor is connected in between BLBBC and VSC. Here a universal bridge is used as VSC. The output of VSC is given to stator phases of BLDC motor, whose output is measured by using measurement port.



ITEE Journal
Information Technology & Electrical Engineering

ISSN: - 2306-708X

Fig. 5. Simulink model of PFC corrected BLDC motor drive.

The Hall Effect sensor gives the position of the rotor, correspondingly the switches of VSC are turned on. This is done using a logic block shown in fig.5. This block will generate the gate pulse to the switches of VSC following the rotor position.

The simulation is carried out by changing the reference speed as well as load torque. The current through the inductor Li1 is continuous in positive half cycle and the current through Li2 is continuous in negative half cycle. This is shown in fig.6. Due to hysteresis controller, iL1 and iL2 vary over a band as shown. In [6], iL1 and iL2 reach zero value in each switching cycle and hence produces more voltage ripples. The DC link voltage shown in fig.6 has a ripple voltage of 2.7V.

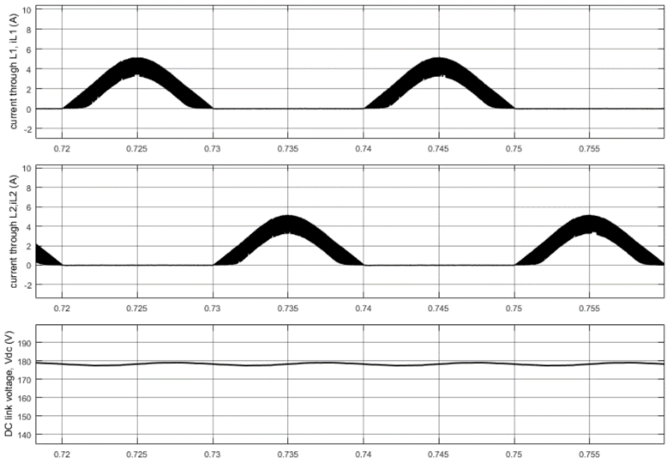


Fig. 6. Waveform of current through inductor Li1, Li2 & DC link voltage.

A. Change in speed reference for a constant load torque

The reference speed is initially 1500 rpm, with a load torque of 1Nm. Corresponding speed and electromagnetic torque waveforms are shown in fig.7.

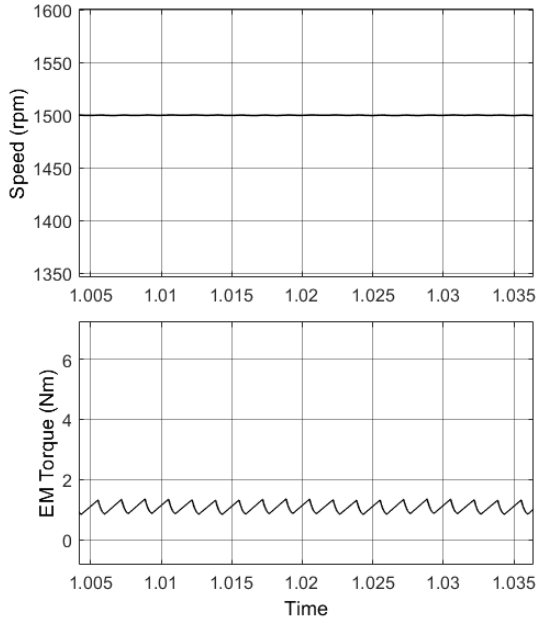


Fig. 7. Waveform of speed and torque for reference speed 1500 rpm.

The speed reaches reference speed (1500 rpm) with a simulation time of 0.6 seconds. Speed settles to 1500 rpm with very small ripple. The stator current and back emf waveforms of BLDC motor are shown in Fig.8.

To validate the closed-loop operation, now speed reference is changed to 1000 rpm without any change in the load torque. The speed transition is shown in fig.9 and eventually settles at 1000 rpm after completing a few oscillations. This transition takes a simulation time of nearly 1 second. Electromagnetic torque also has a transient period but settled down to previous value.

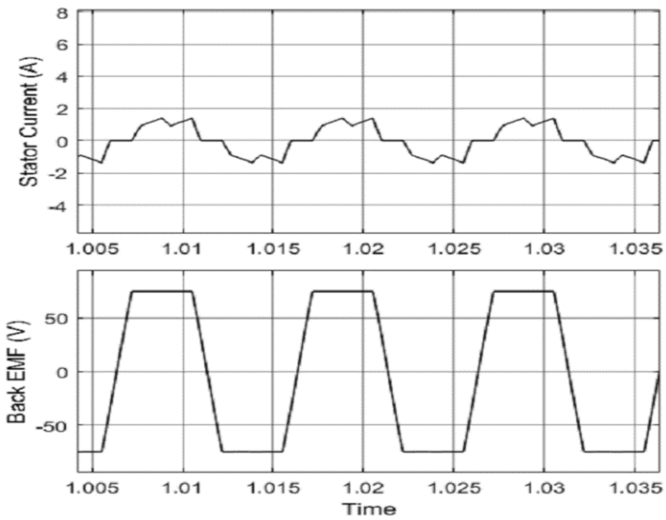


Fig. 8. Waveform of stator current and back emf.

B. Change in load torque while running with a constant speed

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Now the load torque is varied to 1.5 Nm with reference speed of 1500 rpm. This is shown in Fig.10. When load torque increases initially speed decreases, but speed controller bring back the speed to 1500 rpm within 0.4 seconds. This shows that speed control of BLDC motor is effective.

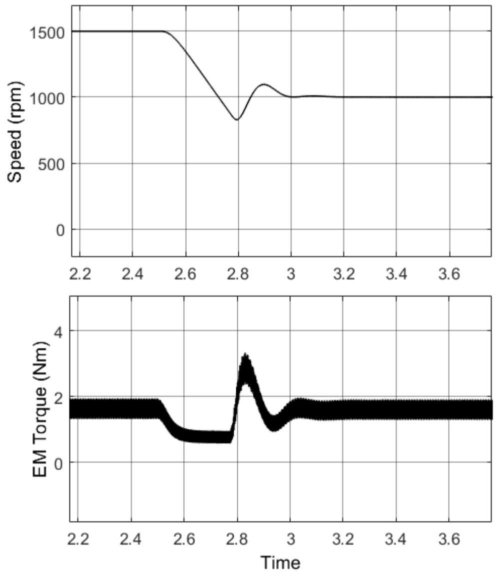

Fig. 9. Speed transition for reference speed change from 1500 rpm to 1000 rpm at a load torque of 1.5 Nm.

The other function of the proposed drive is to make input power factor very close to unity. This can be done by making the input current sinusoidal and in phase with supply voltage. Fig.11 shows the waveforms of input current and input voltage when reference speed is 1500 rpm and load torque is 1.5 Nm. Fig.12 is a scaled version of fig. 11, gives clarity on current and voltage phases. From this, it is found that input current is more or less sinusoidal and in phase with supply voltage. This means the displacement factor is unity. In order to calculate distortion factor, THD value of input current is calculated from FFT analysis tool. The harmonic spectrum is shown in fig.13, and the frequency components are spread over a range due to hysteresis controller.

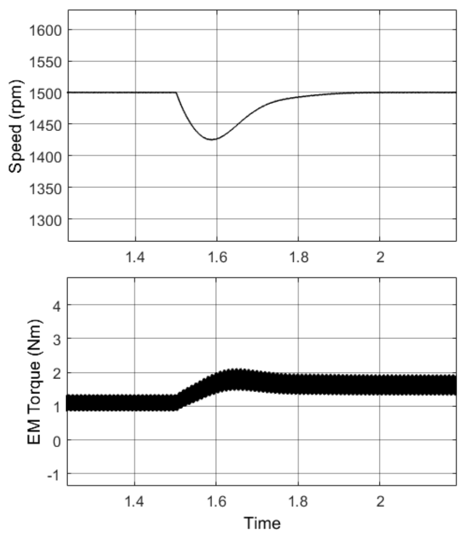

Fig. 10. Speed for change in load torque from 1 Nm to 1.5 Nm with a reference speed 1500 rpm.

From the FFT analysis, the input current THD was found as 4.77%, so the calculated value of distortion factor is 0.9989. Power factor of the proposed drive is 0.9988. The efficiency of the drive is calculated as 84% for a load torque of 1.5 Nm, shown in table 3.

TABLE III

EFFICIENCY AT 1NM AND 1500 RPM

THD (%)	Displacement PF	Power Factor (PF)	Efficiency (%)
4.76	0.99989	0.9988	84%

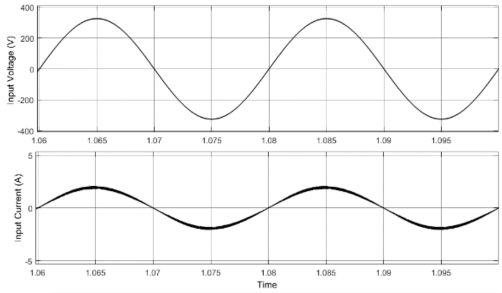

Fig. 11. Input current and input voltage waveforms.

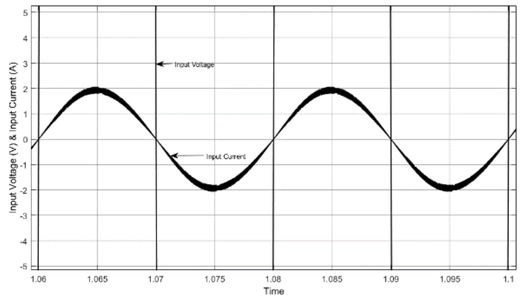

Fig. 12. Input current and input voltage waveforms with in a plot.

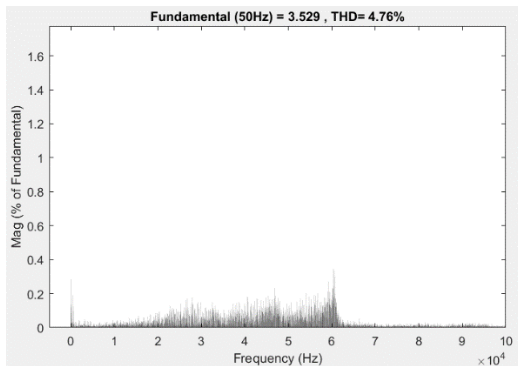

Fig.13. Input current THD using FFT analysis.

6. CONCLUSION

This paper describes a simulink model of a BLDC motor drive with PFC capability. BLBBC converter with a VSC, separated by a dc link capacitor is the main component of the BLDC drive. Hysteresis controller is used to control the

ITEE Journal
Information Technology & Electrical Engineering

ISSN: - 2306-708X

switching pulses of BLBBC. It is clear from the simulation results that inductor currents in BLBBC vary over a small band. Hence, output voltage ripple is reduced which results in reduced speed ripples. Simulation is performed by changing both speed and load torque. Simulation results show the expected performance. The proposed converter is suitable for low power applications with a minimum number of power electronic devices. The power factor of the drive is very much close to unity. The efficiency of the proposed drive is 84% and THD of the input current is within the limit recommended by IEEE standards. The efficiency of the proposed drive can be improved using SiC devices compared to conventional Si devices. Also, when using SiC the switching frequency can be increased, it reduces the size of passive components.

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