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Implementation of Multiplier by CORDIC Algorithm

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ABSTRACT

As we know is present era every multimedia and aerospace based application is require fast processing unit. We also know if any system is complete based on General purpose processor so efficiency of the complete system will be reduce. For application specification there is need of dedicated application specific processor. So here for the aerospace and multimedia application which is based on trigonometric function. So for those kind of application there is need of specific process which is known as CORDIC processor.

Keywords: *SPAA, DCT, ASIC, FPGA, HDL, Algorithm, Architecture.*

1. INTRODUCTION

In computation unit trigonometric features are very essential; at existing many mathematical characteristic require sine, cosine, and tangent and so on, and thru the usage of this set of rules it reachable to compute. With ongoing technology and barriers on energy, walking frequency and strength consumption, if we're generating any trigonometry capabilities by using of multiplier, adder, divider, these architectures consumes more hardware and computational time in-creases, for discount of this trouble cordic set of rules is transformed into hardware structure that is recognized as cordic processor. This processor reduces the hassle of division and multiplication. In cordic processor we can compute the features via the usage of shifter, adder and substractor. In present era cordic set of rules is used in many features like multimedia, digital signal processing. First cordic set of rules [1] is converted into hardware so it was once going thru a few issues like scale element, time ingesting etc. In cordic set of rules many modification is performed but it surely going via many troubles in order for destiny scope this cordic processor require many modification.

2. LITERATURE REVIEW

First CORDIC algorithm is developed in 1959 in this the writer proposed answer for trigonometric attribute and rotation, alternatively this method is going via with many bother like heavy hardware is require, regular time period and scale component is additionally a crucial trouble [1]. An-other new method is developed [2], in this paper writer speak about some new factions like log, exponential and square root however this technique is additionally going thru the same predominant troubles scale factor, giant hardware, regular time period .After the above strategies a lot of enchantment is carried out in cordic algorithm and many generalized method are proposed for computing pretty a variety aspects like sine/cosine [3], [4], transforms [5], [6], exponents/logarithms, rectangular roots, Eigen values [7] etc. During the previous 50 years [8], there have been predominant advances in the format of the algorithm to overcome its predominant drawbacks. In [9], [10], [11] authors advise the use of greedy search algorithms for figuring out the micro-rotations. The effectively of these processes are based totally on the possibility of rotation mind-set which is the important problem. Implementation of it in phrases of hardware is difficult and it's dealing with each other most important problem; variable scale factor. This factor is which reduces the obtain of latency. For bargain of scale difficulty trouble low complexity approach is used and the technique is Taylor sequence increase which moreover has some draw backs. Range of convergence is a most necessary trouble ,for Reduction of this hassle some new strategy is suggested. The low complexity technique for getting rid of the scale thing is the use of Taylor sequence expansion. The Scaling-Free CORDIC and modified scale-free CORDIC[12], [13] are techniques based totally on Taylor sequence approach. The former suffers from low differ of convergence (RoC) which renders it unsuitable for realistic applications, even as the latter extends the RoC then again them dealing with problem of regular scale-factor of $1/\sqrt{2}$. The Scaling-Free CORDIC and modified scale-free CORDIC [14, 15] in [14] author suggested new technique for technology of sine/cosine, in this method creator take away a ROM and a large barrel shifter in the hardware implementation of the CORDIC system, alternatively this strategy suffers from low differ of convergence (RoC) which render take a seat down unsuitable for sensible applications, in [15] creator proposed one new approach for bargain of scale element and extent of iterations. They focused on Radix-4 Modified Booth Recording- Modification of CORDIC algorithm is Radix-4 modified income area recording, with this it continues working barring a scale element and the corresponding hardware for statistics route can nevertheless be excluded, whilst enabling

each and every technology in pipeline stage which approach two bits at a time from the vector. By this creator reap bargain in quantity of iterations. Constant multiplier-there is one steady time length is produce which is $1/\sqrt{2}$ for this steady time length in previous works extra hardware is require, so this can be avoided with the useful resource of ordinary multiplier which is restrict greater hardware problem. Domain Folding Elimination, In preceding work perspective of the scaling-free CORDIC kernel is between zero to $\pi/8$ rad alternatively in this work convergence vary is between $-\pi/2$ to $\pi/2$,[14],[15] additionally dealing with consistent scale issue problem. In [18] right here creator propose the leading-one bit detection approach to discover the micro-rotations. The scale free sketch of the proposed algorithm is notably primarily based on Taylor sequence growth of the sine and cosine waves. In [19] writer use the same approach alternatively there they implement Hyperbolic cordic function. A hardware environment pleasant structure for producing SINE and COSINE waves based totally definitely on the CORDIC (Coordinate Rotation Digital Computer) algorithm. [16].this advocated a novel strategy in this approach creator makes use of leading-one bit detection technique to pick out the micro-rotations. This manner dispose of intricate search algorithm. The scale free sketch of the algorithm is principally based totally on Taylor sequence growth of the sine and cosine waves. This proposed algorithm is up to fourth order of Taylor series. Micro-Rotation Sequence Generation, in preceding work for point of view rotation ROM is required alternatively via the usage of the usage of Micro Rotation Sequence Generation no any ROM require for storing the primary angles of rotation. This proposed algorithm is additionally dealing with many problems like extend in error, broad variety of new release increases, to reduce this trouble each and every different technique is recommended [17]. In this method creator the use of equal strategy of [16]but they convert that shape in to parallel shape they proposed CORDIC parallel rotator implementation to be maximally optimized for immoderate standard overall performance with the reduce price in area-consuming.

Basic Cordic Algorithm:

Cordic set of rules [1] the underlying principle of the cordic set of rules is primarily based usually on -measurement geometry. This set of regulations operates each and each and every in or rotation or vectoring mode, following linear, round or hyperbolic trajectories. We focal trouble on rotation mode of operation in spherical trajectory. A. Traditional cordic algorithm permit the vector va[xa, yb] be derived through rotating the vector vb[xayb] by using potential of using manner of an nation of mind Θ,then:

$$\begin{bmatrix}\mathrm{Xb}\\ \mathrm{Yb}\end{bmatrix} = \mathrm{Rp}.\begin{bmatrix}\mathrm{Xa}\\ \mathrm{Ya}\end{bmatrix}, \mathrm{Rp} = \begin{bmatrix}\mathrm{Cos}\theta & -\mathrm{Sin}\theta\\ \mathrm{Sin}\theta & \mathrm{Cos}\theta\end{bmatrix} \quad (1)$$

Equation (1) varieties the essential precept for iterative coordinate calculation in cordic set of rules [1]. The important thing belief in understanding rotations using cordic is to express the angle of rotation θ as an aggregation of pre-described fundamental angles described as: the vicinity b is the word-length in bits. (2)

$$\theta = \sum_{I=0}^{B} \mathrm{ui} * \mathrm{ai} \quad (2)$$

The roc of the traditional cordic is [−99. 9o, 99.9o] and the use of more iteration step can be prolonged to the whole coordinate space. The rotation matrix rp, in its special shape is computation in depth; it requires computing sine and cosine competencies with four multiplication and two addition operations. Factoring the cosine time duration simplifies the Rotation matrix rp (1) via the usage of changing the multiplication to shift operations, as tangent of the primary angles is described in terrible powers of (2). However the penalty paid is the advent of the scale-factor which varies in accordance to the cosine of the essential-rotation. As considered from (3), the measurement element ki is independent of the path of micro-rotation. With sequential execution of large form of iterations it has a tendency to a constant, referred to as the achieve of the cordic set of rules. The size-factor is as a final result compensated each internal the submit or preprocessing unit.

$$\mathrm{Rp} = \mathrm{Ki}.\begin{bmatrix}1 & -\mathrm{ui}.2^{-\mathrm{i}}\theta\\ \mathrm{ui}.2^{-\mathrm{i}} & \mathrm{Cos}\theta\end{bmatrix} \quad (3)$$

Scaling-unfastened cordic [12] used to be the most attempt to cartoon scale-loose coordinate cordic equations the utilization of taylor collection boom. Proper right here, the micro-rotations are limited to anti-clockwise route handiest, such that, any attitude of rotation is represented because the algebraic sum of quintessential angles. The sine and cosine factors are approximated.

3. THE WALLACE TREE MULTIPLIER

The wallace tree multiplier is significantly quicker than a clean array multiplier due to the fact of the truth its top is logarithmic in phrase duration, now not linear. But, in addition to the giant big sort of adders required, the wallace tree's wiring is an awesome deal a lot loads a lot less normal and larger complicated. As a stop result, wallace timber are frequently averted through designers, on the same time as design complexity is a hassle to them.

Wallace tree styles use a log-depth tree community for discount. Faster, however abnormal, they exchange ease of layout for velocity. Wallace tree styles are commonly prevented for low electrical strength programs, thinking about that more of wiring is likely to consume extra electricity. While subsequently quicker than bring-shop shape for massive bit multipliers, the wallace tree multiplier has the drawback of being very abnormal, which complicates the mission of coming with an environment exceptional layout.

The wallace tree multiplier is an excessive tempo multiplier. The summing of the partial product bits in parallel the usage of a tree of deliver-preserve adders grew to turn out to be oftentimes diagnosed due to the fact of the fact the "wallace tree". Three step methods are used to multiply numbers Establishment of bit products, Discount of the bit product matrix right into a two row matrix by means of capability of a elevate shop adder, summation of remaining rows the usage of a faster lift look beforehand adder (cla).

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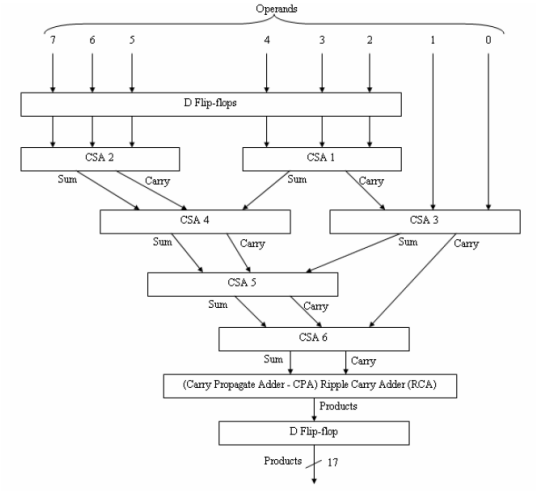

Fig.1 Wallace tree Multiplier

4. THE BOOTH'S MULTIPLIER

Even though wallace tree multipliers have been faster than the ordinary furnish keep technique, it moreover modified into as quickly as very bizarre and as an end result grew to come to be into as rapidly as tough at the equal time as drawing the layouts. Slowly at the same time as multiplier bits receives preceding 32-bits massive numbers of frequent revel in gates are required and for that purpose in addition greater interconnecting wires which makes chip structure huge and slows down working tempo sales area multiplier can be used in one-of-a-type modes collectively with radix-2, radix-4, radix-8 and so forth. But we decided to apply radix-4 salary area's set of policies due to the reality of range of partial merchandise is diminished to n/2.

4.1 Implementation of Radix-4

One of the picks for recognizing excited velocity multipliers is to beautify the similarity that helps limit the large form of the subsequent calculation steps. The unique version of the Booth multiplier (Radix - 2) had drawbacks. The huge kind of upload / subtract operations grew to emerge as variable and because of this grew to come to be inconvenient even as designing parallel multipliers. The set of insurance policies will flip out to be inefficient at the equal time as there are isolated 1s.

The ones troubles are conquering through using radix four earnings space's algorithm which can scan strings of three bits with the set of suggestions given underneath. The layout of booth's multiplier in this mission consists of 4 modified sales region encoded (mbe), 4 signal extension corrector, four partial product mills (accommodates of 5:1 multiplexer) and as a give up end result a wallace tree adder.

This earnings neighborhood multiplier technique is to make greater tempo via decreasing the giant trend of partial merchandise thru potential of manner of 1/2. Whilst you reflect on consideration on that an 8-bit profits region multiplier is used on this project, so there are completely 4 partial products that desire to be delivered as chance of eight partial merchandise generated the usage of everyday multiplier. The shape sketch for the changed cubicles set of guidelines used in this mission.

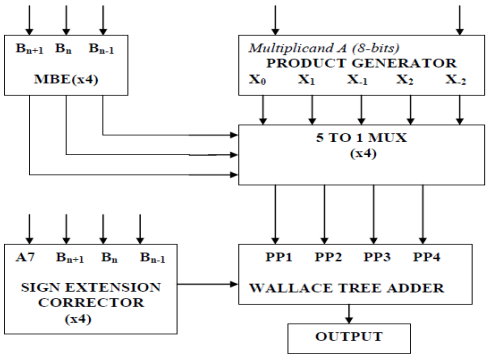

Fig.2 Architecture of Booth Multiplier

5. MODIFIED BOOTH MULRIPLIER

Modified sales space encoding is most regularly used to keep away from variable dimension partial product arrays. Earlier than designing a mbe, the multiplier b must be converted right into a radix-four quantity with the aid of dividing them into three digits respectively in accordance to sales space encoder desk given afterwards. Prior to transform the multiplier, a zero is appended into the least tremendous bit (lsb) of the multiplier. The figure above shows that the multiplier has been divided into four partitions and hence that mean four partial products will be generated using booth multiplier approach I instead of eight partial products being generated using conventional multiplier. Zn = -2* Bn+1 + Bn + Bn-1 Lets take an example of converting an 8-bit number into a Radix-4 number. Let the number be -36 = 1 1 0 1 1 1 0 0. Now we have to append a '0' to the LSB. Hence the new number becomes a 9-digit number, that is 1 1 0 1 1 1 0 0 0. This is now further encoded into Radix-4 numbers according to the following given table. Starting from right we have 0*Multiplicand, -1*Multiplicand, 2*Multiplicand, -1*Multiplicand.

Table 5.1 Analysis of Multiplicand

B_{n+1}	B_n	B_{n-1}	Z_n	Partial Product	1M	2M	3M
0	0	0	0	0	1	1	0
0	0	1	1	1×Multiplicand	0	1	0
0	1	0	1	1×Multiplicand	0	1	0
0	1	1	2	2×Multiplicand	1	0	0
1	0	0	-2	-2×Multiplicand	1	0	1
1	0	1	-1	-1×Multiplicand	0	1	1
1	1	0	-1	-1×Multiplicand	0	1	1
1	1	1	0	0	1	1	0

This Table shows Bn+1, Bn and Bn-1 which are three bits wide binary numbers of the multiplier Bin which Bn+1 is the most significant bit (MSB) and Bn-1 is the least significant bit (LSB). Zn is representing the Radix-4 number of the 3-bit binary multiplier number. For example, if the 3-bit multiplier value is "111", so it means that multiplicand A will be 0.And it's the same for others either to multiply the multiplicand by -1, -2 and so on depending on 3 digit number. And thing to note is generated numbers are all of 9-bit.

5.1 Tree Multiplier

According to [13] author used existing Wallace tree method but the use the small size full adder which will reduce the hardware consumption.

This architecture reduces the partial products at a rate of log 3 2 (N 2). Figure shows an example of tree reduction for an 8*8-bit partial product tree. The ovals around the dots represent either a full adder (for three circled dots) or a half adder (For two circled dots). This tree is reduced to two rows for a carry-propagate adder after four stages. There are many ways to reduce this tree with CSAs, and this example is just one of them.

6. RESEARCH GAPS

Scaling and hardware complexity are main difficulty but latency also create some issues about the speed. This method reduces latency problem but despite the fact that we will lower latency in term of hardware.

6.1 Application

There are many applications where we have to use cordic processor and those applications are:

- Aerospace Application.
- Discrete Cosine Transform (Image Compression Unit).
- Different DSP and DIP Filters.
- Multimedia Applications.

6.2 Required Software Tools

This Paper will develop in both level means algorithm and architecture level. So for algorithm level we will use matlab and application level analysis will be perom on DCT by using of Matlab. Simmilar architecture level design will be done on Xilinx and verification will be done on Modelsim.

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Table 6.3 Software Tools Summary

Development Tools (Algorithm)	MATLAB Version 11
Development Tools (Arhitecture)	Xilinx ISE Version 14.
Simulation & Verification Tool	ModelSim 8.1 and Matlab

7. PROPOSED IMLEMENTATION

Here we will propose a novel architecture of Cordic Processing Unit with the motto of reducing the time complexity & scale factor issue at algorithm level. Similar at architecture level we will make justification with SPAA metrics according to out paper theme. According to that concept we will design fast algorithm and we will reduce the time complexity. After that we will design architecture of processing unit by using of our propose Cordic algorithm. At initial stage we will design our own novel algorithm after that we will design of our architecture of propose novel algorithm. Now for analysis point of view we will use DCT as an application where we will apply our proposed logic with previous existing logic. There we will compare the output image quality with different image quality parameters. Now at hardware stage we will use Verilog HDL and design our architecture on Xilinx 14.2. Virtually we will do analysis on Vertix 6 FPGA. Using verilog verification we will Check the efficiency of our propose design.

8. CONCLUSION

This paper added a way to extend the enter differ of the cordic ip cores on hand in fpgas. Because of the fact exponential characteristic is a truly regularly used one in a few of the dsp particularly primarily based definitely sincerely applications, this cool lively film will discover out software program application utility software program in areas of signal processing, photograph processing. It is able to moreover in addition be utilized in rising region of neuron-prosthetic studies, the vicinity the biologically inspired neuron fashions have mathematical equations coping with exponential of large values. The structure simulation penalties very intently matched the expected values calculated the utilization of matlab. The layout modified into as speedy as synthesized and mapped to xilinx fpga and tested. A couple of instantiations of the format module had been effectively utilized in a software program for the fpga implementation of a hodgkin huxley model of a single neuron.

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